HDP User Group International, Inc.
Underfill Process Guideline

Date of Presentation: February 24, 2010

This project is in the **Definition Stage**
Project Lead:
Po Tse : Philips Healthcare
Co-lead by: Steve Hugh, Philips Healthcare (AED)

Background

- **High reliability industries require significant testing and rationale for adopting Pb-free processing due to mission criticality and field life requirements**
- **Recent investigations have shown that Pb-free solder joints for BGA's and CSP's are robust in standard thermal cycling fatigue life testing, but insufficient testing has been conducted to understand field behavior**
- **Other work has shown that Pb-free alloys significantly reduce the mechanical shock endurance of Pb-free BGA and CSP assemblies**

Background

- **Underfill is widely recommended to strengthen Pb-free solder joints during both thermal cycling and mechanical shock environments**
- **The method of selecting underfill materials for specific applications and environments is not well understood. This drives issues of**
  - **Compromised reliability**
  - **Unnecessary costs**
- **Previous work such as J-STD-030 addresses processing, testing, and acceptance but not reliability and costs**

Purpose

This project will determine the parameters for selecting cost-effective underfill mitigation for the reliability improvement of Pb-free assemblies.

The project will:

- Deliver information focused on selection, testing and optimization of an underfill material for BGA's, CSP's and other components.
- Provide modeling of materials and lifetime models to help predict when to use underfill.
- The results of this project will impact the medical, automotive, telecom, and other high reliability industries.
- A final report will be issued upon project completion.

Goals and Objectives

- Develop algorithms and models for determining correct underfill materials and best candidates for Pb-free underfill operations to be used for BGA's, CSP's, QFN's and other leadless components.
- Identify optimal reliability test criteria (ATC, vibe, drop, shock, aging, humidity etc.).
- Determine effect of application methods for underfill materials (corner bond and complete underfill).
- Determine reliability of various underfill application methods as well as component size cross-over point for underfill/no underfill.

Some Process/Reliability Tradeoffs

- **Reworkability**

  Ability of the material to allow removal and replacement of the bonded component. Usually means a lower glass transition temperature, lower cure temperature, and lower modulus.

- **Cure temperature**

  A lower temp cure cycle will cause less thermal damage to components on the circuit board. Some components, esp. flash memory and other programmed devices can loose programming at high temperatures. Some types of capacitors are esp. susceptible to temperature – either the dielectric materials are sensitive to heating or the construction such as film caps will not take higher cure temperatures.

- **Modulus and Coefficient of Thermal Expansion**

  Higher modulus materials (>1GPa) – i.e. materials containing more filler are shown experimentally to prolong the life of the components in thermal cycling than those bonded with lower modulus materials. There is some concern that high modulus underfills could have detrimental effects due to CTE mismatch between bonding surfaces (solder mask and components. These higher filled materials also tend to have higher glass transition and higher cure temperatures.

- **Humidity**

  Underfill materials can change properties in humid environments

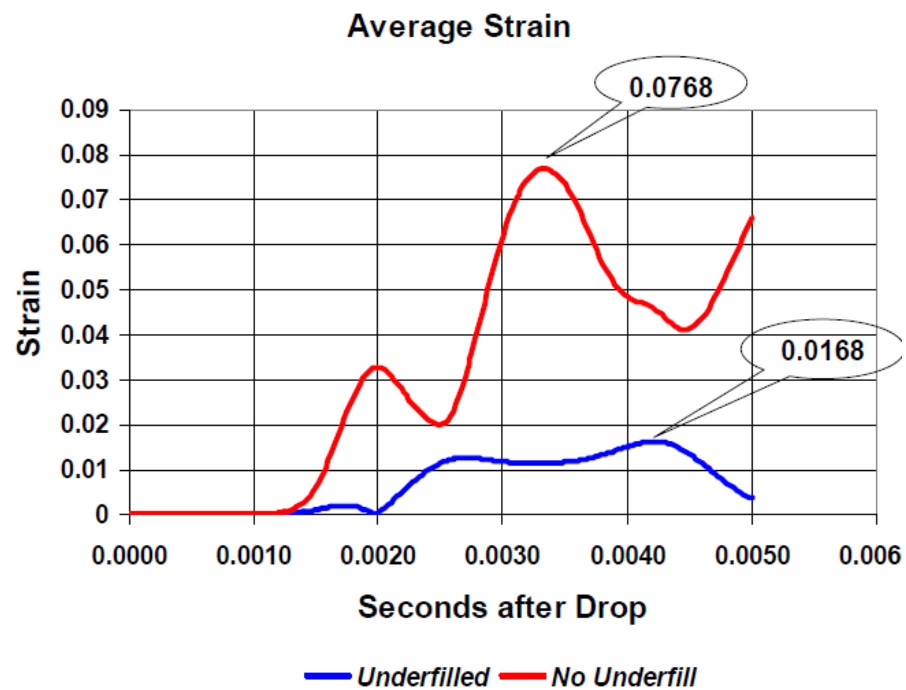
Progress since October 2009

- Literature survey – COMPLETE
  - Reviewed abstracts, papers provided focus
  - Asymtek paper by Steven Adamson – good summary
- Understand use environments – HDPUG members, others – COMPLETE
  - Decision to make model that supports wide OEM applicability
  - Entry point to model is board strain – requires some testing to retrieve this value
- Enlist expertise in finite element modeling – COMPLETE
  - DfR Solutions has previous modeling expertise for NAVY
  - Nathan Blattau, Craig Hillman active participants

Finite Element SOW

Model inputs

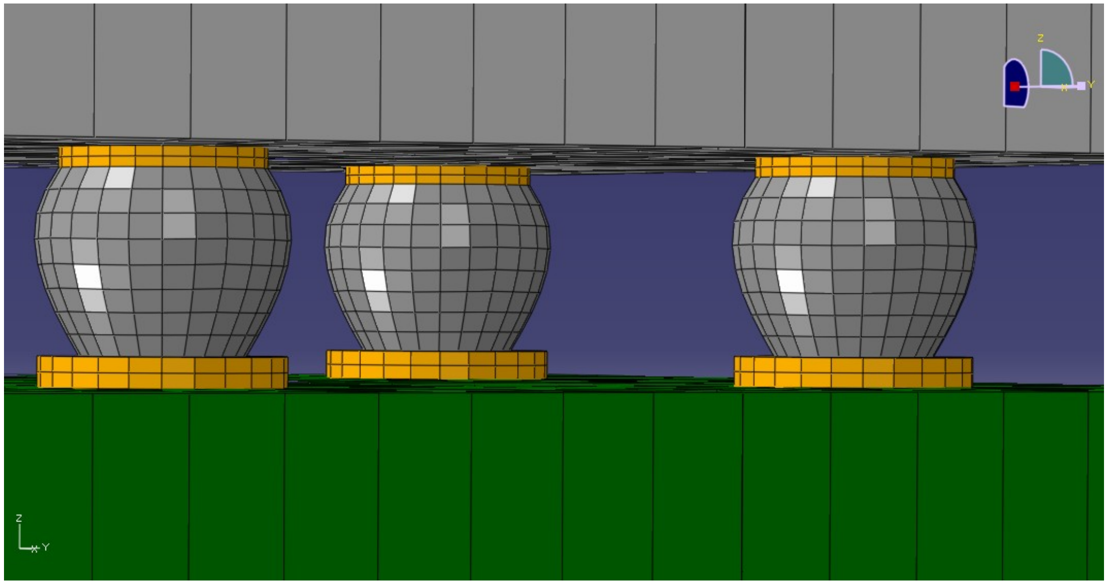
- Board level strain
  - This provides a generic entry point for users into the model. Users derive the strain number as follows:
  - Attach strain gauge to board near perimeter of BGA's
    - Measure strain during drop
    - Measure strain during vibration
- Package geometric parameters
  - Die size
  - BGA substrate thickness
  - Ball diameter
  - Number of connections to board



From: Steven Adamson - Asymtek

Finite Element SOW

- Model inputs (continued)
  - Package material properties
    - Package modulus
    - Molding type
    - Solder
  - Package to board solder type
  - Geometry of underfill
    - Corner stake
    - Full underfill



DfR Solutions – Craig Hillman and Nathan Blattau

Finite Element SOW

- Model inputs (continued)
  - Material properties of underfill
    - Modulus
    - CTE
    - Adherence to board solder mask and to package
    - Cure shrinkage (stress free temperature)
    - Tg glass transition temperature
  - Board parameters
    - Number of layers
    - Type of layers - signal, ground
    - Laminate types
    - Thickness of layers

Finite Element SOW

- Model outputs
  - Mechanical shock failure prediction
    - Probability of a certain shock level causing a failure event
  - Thermal cycle life prediction
    - Based on Weibull slope - Usually expressed as cycles to .1 or 1% failure

Progress since October 2009

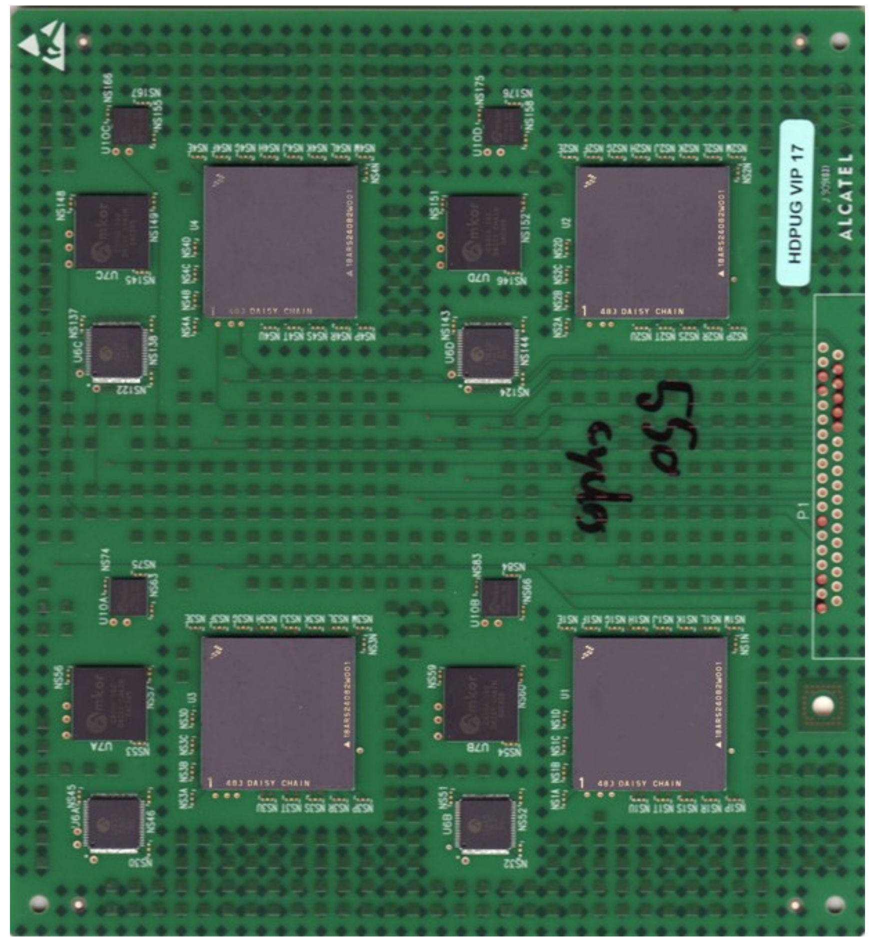
- Focus session on DOE with underfill suppliers on materials and tradeoffs – COMPLETE
  - DOE planning
  - More thought required about results/analysis at the end point… targeting a probability distribution

- Leverage test vehicles and plans from previous Pb-free HDPUG studies – IN PROCESS
  - Mechanical shock vehicle vs. thermal shock vehicle
  - Combined test vehicle – mechanical/thermal
  - Sharing test vehicle among projects

DOE / Test Vehicle

Modified Via-In-Pad from HDPUG study

- Change component locations so they are symmetrical about the center of the board
- Remove vias-in-pad from 1/2 the parts that currently have them
- Support dual board thickness: .062 and .125 inches
- Place additional connector opposite current connector to balance mass and stiffness
- Laminate type: Polyclad 370HR



DOE / Test Vehicle

Given

- Package geometry - as per Via-In-Pad test vehicle
- Package to board solder type - SAC305
- Board parameters
  - Laminate type
  - Number of layers

DOE / Test Vehicle

- Variables for modeling and test vehicle build
  - Board strain
    - .062 and .125 board thickness – creates distinct strain levels
    - Place strain gages near BGA groups (4), in center of board, and near standoff's and then dropping the boards
  - Geometry of underfill
    - Corner stake
    - Full capillary
    - Fluxing underfill (Indium) - Soft only
  - Underfill material
    - Soft: <1GPa
    - Medium: 3-5 GPa
    - Hard: approx 10 GPa

DOE / Test Vehicle

- Responses
  - Cross-section of each board type so accurate data on underfill geometry can be used in the model
  - Strain and accelerometer measurement for representative board(s)
  - Number of drops to component failure
  - Number of cycles to component failure

DOE / Test Vehicle

- Challenges
  - Reduce variables and increase sample size to focus on enough data for a failure probability distribution
  - If we go for the whole matrix, for each board thickness….

	Soft	Medium	Hard
Full capillary	x	x	x
Corner stake	x	x	x
Fluxing	x		

  - 2 board thickness x 7 combinations x 20 replicates = 280 boards for each response –> 280 for drop test, and 280 for thermal cycle!!

DOE Ideas

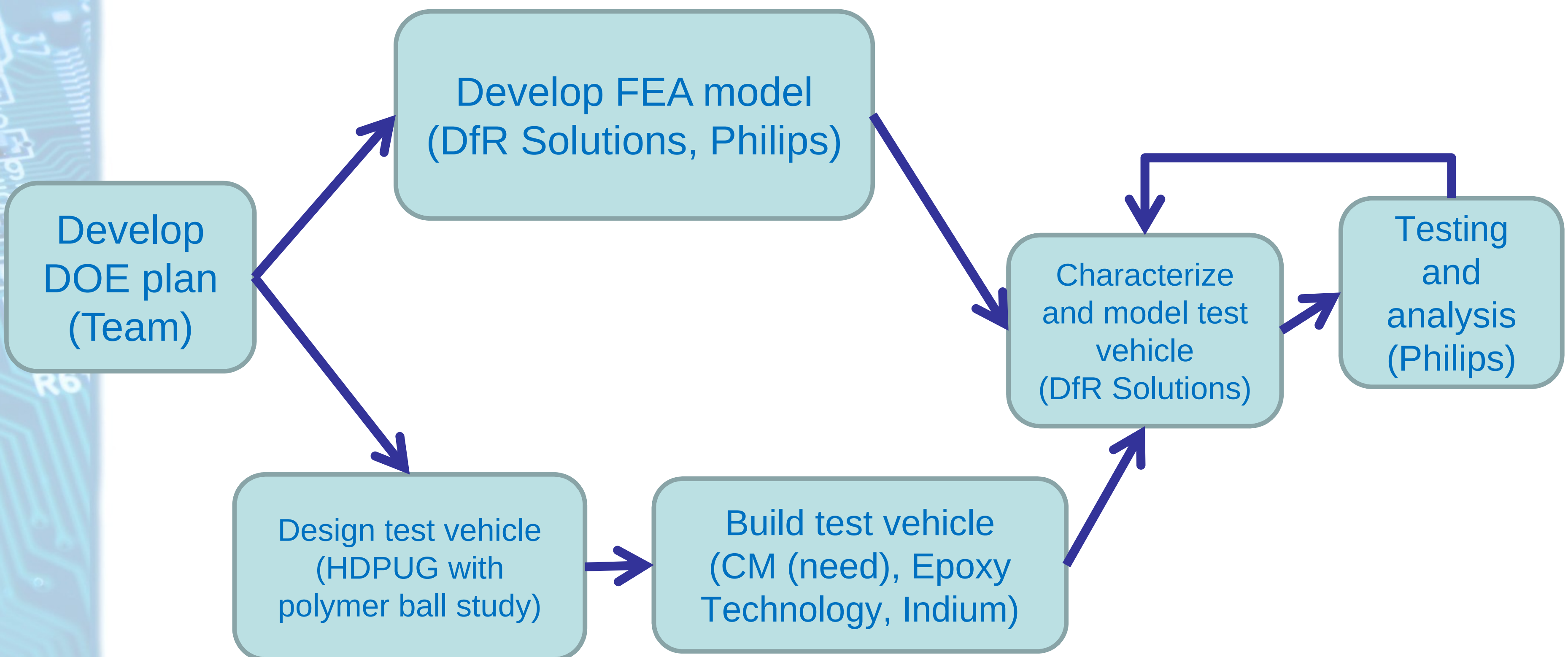
- Reduce variables, conditions, replicates

	Soft	Medium	Hard
Full capillary	20	20	20
Corner stake	20	20	20
Fluxing	20		

- Build one leg of experiment at a time to check feasibility
  - The engineering approach

- Others?

Resources/Project Flow



Project Execution Plan

Project Task (Activities are examples)	When Complete	Actual (Implementation Stage only)
Plan Project	Feb 2010	Date/Month/YY
Create preliminary analytical model and test plan	Apr 2010	Date/Month/YY
Board design/verification	Apr 2010	Date/Month/YY
Approval by project members	May 2010	Date/Month/YY
All components received	Jul 2010	Date/Month/YY
Fabricate and electrically test boards	Aug 2010	Date/Month/YY
Assemble & inspect boards	Sep 2010	Date/Month/YY
Testing – Drop/Shock, Temp cycle, etc.	Dec 2010	Date/Month/YY
Failure Analysis	Jan 2011	Date/Month/YY
Verify and/or refine analytical model	Feb 2011	Date/Month/YY
Complete Project Report	Apr 2011	Date/Month/YY
Publish report to HDP Membership	Apr 2011	Date/Month/YY

Team Members

- Asymtek (Steven Adamson)
- DfR Solutions (Craig Hillman, Nathan Blattau)
- Epoxy Technology (Joe McCabe)
- Indium (Dr. Ning-Cheng Lee)
- Philips (Po Tse, Steve Hugh, Jerry Purnell)
- Sunstar Engineering (Steven Edward)
- Venture (Vincent Liu)
- Zymet (Karl Loh)

- Project Co-leader: Po Tse, Steve Hugh
- Project Facilitator: Laurence Schultz