

# 3D Interconnect Technology Needs and Issues Analysis

## HDPUG Questionnaire

HDPUG Facilitator  
Project Proposal

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# Questionnaire availability



- Attached questionnaire on interest in 3D Packaging is sent to HDPUG Members and some potential participants, mainly suppliers or customers of Members
- Filling in the questionnaire comprises no agreement to participate
- Non-members can also participate in discussions on project proposals
- Only when a planned project is taken to Implementation is Membership necessary

# Goals of this Questionnaire



- Identify one or more technology and/or reliability topics in existing and emerging 3D technologies for experimental assessment by HDPUG
- Focus is on supply chain management of electronics packaging industry, collecting different views on drivers and key issues
- Members are encouraged to forward a copy of the questionnaire to their suppliers and customers
- Both long existing commercial products and newly published ideas can be included, as long as they are public and the respondents see a need for cooperative work

# Project Proposal Background



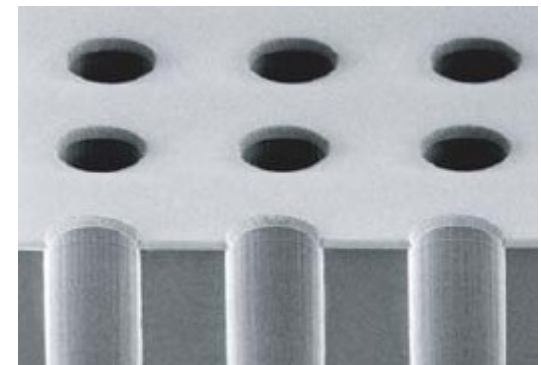
- Conceived in June/July 2008 by Semiconductor Packaging work group as an embedded chip demonstrator bundled with:
  - Investigating the impacts of 3D die-stacking, wafer stacking, TSV & other ICT methods
  - Embedded & stacked ICs for processor, subsystem & RF module applications
  - Embedded capacitors and/or Passive Integrated Devices for Packaging/SiP applications
  - High Temperature packaging/thermal packaging
  - Micro QFN reliability
- Preliminary proposal Oct 2008 for micro QFN & embedded die SiP
- Moved to definition stage Nov/Dec 2008 :
  - WiMax embedded IC SiP demonstrator for performance/reliability testing
  - Option for embedded PIDs
  - 3D SiP Technology Guideline
- Project stopped 2009-Q2 due to demonstrator not available
- Restart November 2009: Re-do a comprehensive questionnaire on 3D SiP and interconnect detailed needs, alternative solutions and above all COMMON ISSUES TO ASSESS TOGETHER IN THE SUPPLY CHAIN

# 3D Packaging Guideline



## Focus on commercially available technologies

- Enlarge scope of questionnaire to include 3D technology from all sectors
  - Systems : top-down design drivers – why/how to use 3D - architecture
  - IC Foundry : stacking (die/die, wafer/wafer) micro fabrication (TSV, PIDs, Si interposers)
  - Foundry Back-end : redistribution/WLP, bumping, pillars,
  - Packaging : die stacking, embedding, PoP, CoG, ICT methods (WB, FC, ACF, etc)
  - Substrate + PCB : passive/IC embedding, UT-CSP/PoP, thermal solutions, 3D mold/fold
  - Assembly + Test : COB, PCBA stacking, thermal modules, up-stream die attach, KGD + test
- Include in each section:
  - Key issues from system/component design perspective
  - Design/fabrication methods/features
  - Benefits/detriments/trade-offs/alternatives
  - Diagrams/illustrations/photos as appropriate
- Need:
  - 1 champion, 1~2 collaborators per section



Through Silicon Vias - Silex  
*Extending IC Fab + Package to 3D*

# 3D Packaging Guideline Cont.



## **Some technologies to be assessed and potentially included:**

- Multichip solutions: MCM-L MCM-C MCM-D
- POP Package on Package
- Embedded passives and IPD
- Stacked dies & Embedded dies
- Flex based solutions vs. TSV (Through Silicon Via)
- Module to board attach

## **Engineering and business issues:**

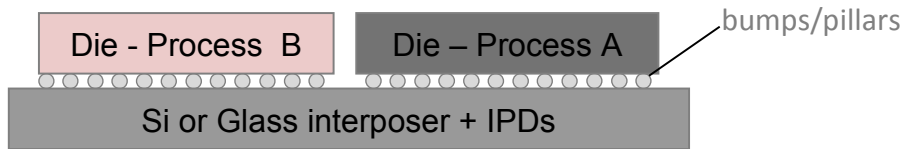
- KGD (Known Good Die) issues
- Module subcontracting
- Supply chain issues (availability, responsibility, technology compatibility)
- Cost structure, cost of ownership
- Reliability
- More than Moore (getting the semiconductor industry involved)

## Example – Semiconductor Device Drivers

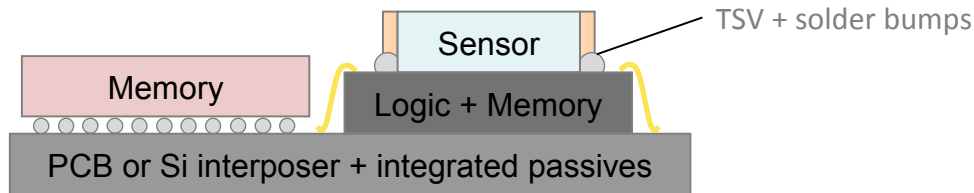
IC Segment	Conventional Fab Problems	3D Fab Solutions
General	Declining returns on design rule shrink	Re-order spatial relationships & increase areal density
Microprocessors	Wire length limits speed	Shorten wires to reduce delays
	CMOS process below 32nm uncertain	Stack transistors for faster CMOS
High Capacity Flash	Unstable operation at/below 32nm limits design rules/die shirk	Increase areal density by die-stacking in proven process node
	Poor process yield below 32nm, diminishing returns	Optimize yield using proven technology
High Capacity DRAM	Wire length limits speed	Stack with TSV or bumps, eliminate or shorten wires
	Declining opportunity to reduce capacitor size/design rules	Increase areal density by die-stacking, no need to reduce capacitor size
Memory/Logic/SoC/Si P/ Optical	Conflicting process/material/design rule requirements	Integrate chips from different processes
	Declining cost reduction of process node generations (below 65nm)	Stacking cheaper in some cases
	Miniaturization/integration	Stacking enables SiP modularization (eg, RF/sensor/logic/memory, optical)

## Example – Logic + Mixed Signal

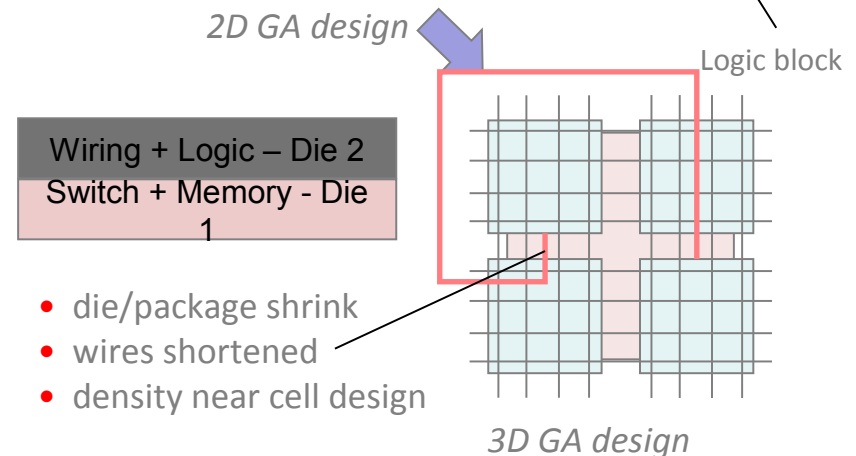
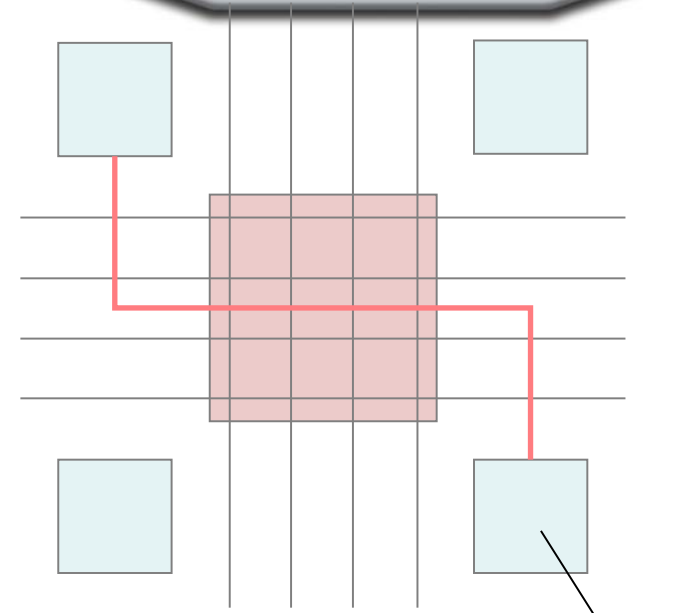
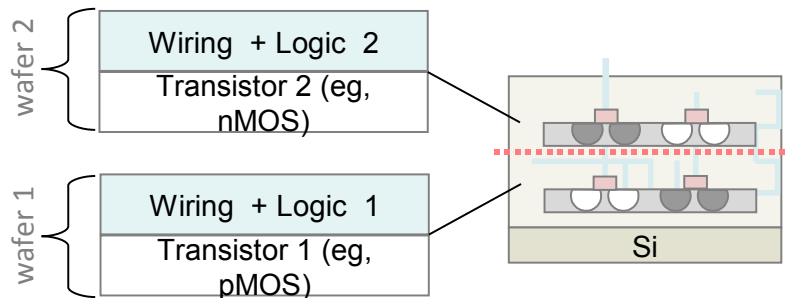
Combine dies from different processes/materials



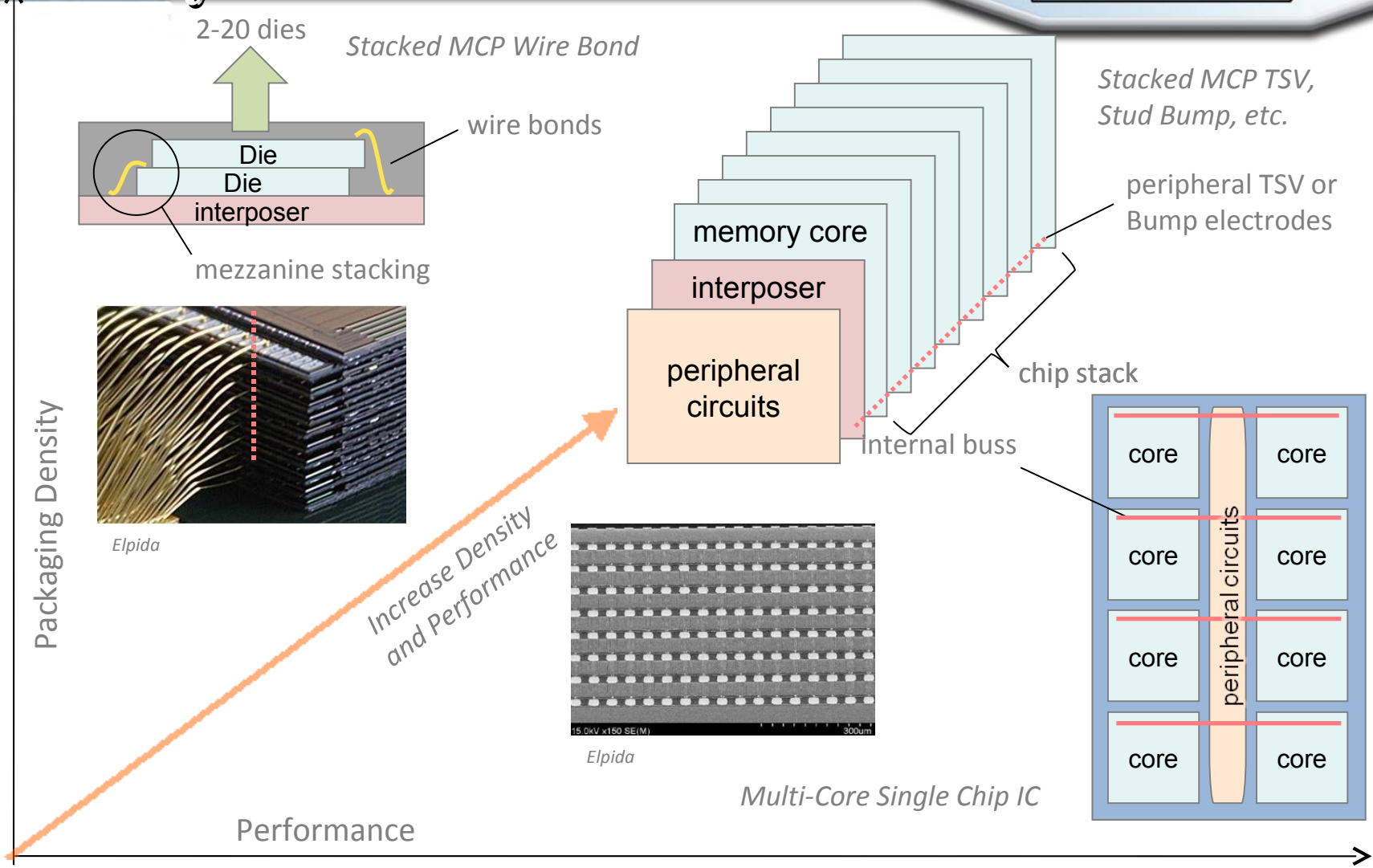
Combine dies to create System in Package modules



Compound Wafer Fab to Optimize Performance/Density



# Example – High Speed/High Density Memory





# Questionnaire on Technology Issues

- Questions and format to be agreed in workgroup
- Sent out before end of 2009, replies within January 2010
- Focus on respondent's perceived issues on 3D SiP implementation
- Goal: Find common issues awaiting supply chain joint solution

HDP Users Group - 3D Technology Member Survey

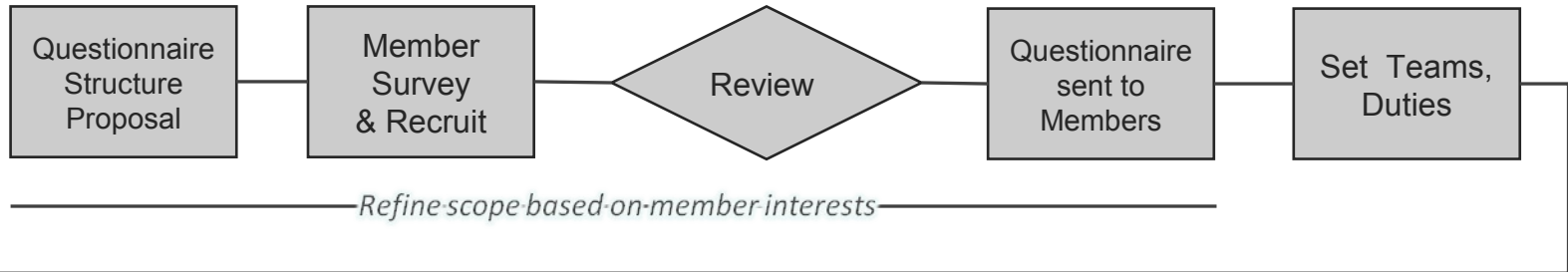
Company :  
 Contact :  
 e-mail :

Item	Technology/Topic	Interest Level	Specific Issues / Remarks	Follow-up
		0 - 3		
1.0	3D - General Applications			
1.1	High Speed Logic			
1.2	High Speed/High Capacity Memory			
1.3	Flash Memory			
1.4	Logic/Memory Integration (including multiple die solutions)			
1.5	Mixed Signal/RF Integration (incl. mixed die Si/Gas, baseband/logic, etc)			
1.6	System in Package - Logic			
1.7	System in Package - RF Subsystems (eg. Bluetooth, WiFi, WiMax, etc)			
1.8	System in Package - Sensor Subsystems (eg. cameras, accelerometers, thermosensors, etc.)			

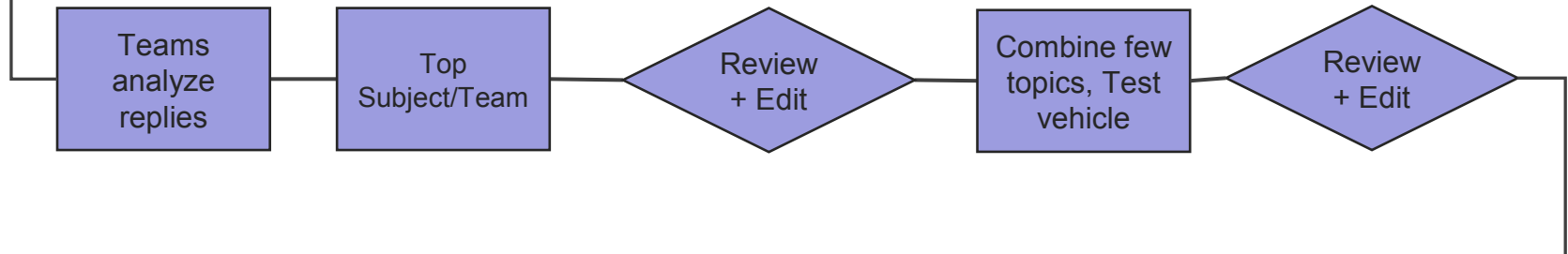
# Analysis Project Workflow



Preparation & Planning *(complete end 2009)*



Active Analysis Project *(Q1 2010)*



February 2010 Member Meeting in San Jose

