

The logo for HDP (High Density Packaging) is displayed in a blue, serif font. It is positioned above a white rectangular box that contains the text 'USER GROUP INTERNATIONAL, INC.®' in a blue, sans-serif font. The entire logo is set against a light blue background that has a decorative, elongated shape.

USER GROUP
INTERNATIONAL, INC.®

3D SiP project planning

Project suggestions

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3D Mission Statements



- Performance & Reliability Assessment
- Collect & analyze data
- Viability for High Reliability Applications (Medical, Telecom)
- Cost analysis for viability of suggested construction
- Suggest 2-4 test vehicles to cover the target applications
- 3 models of organic substrates
- 1 model of stacked die on Si TSV interposer

3D List of project topics



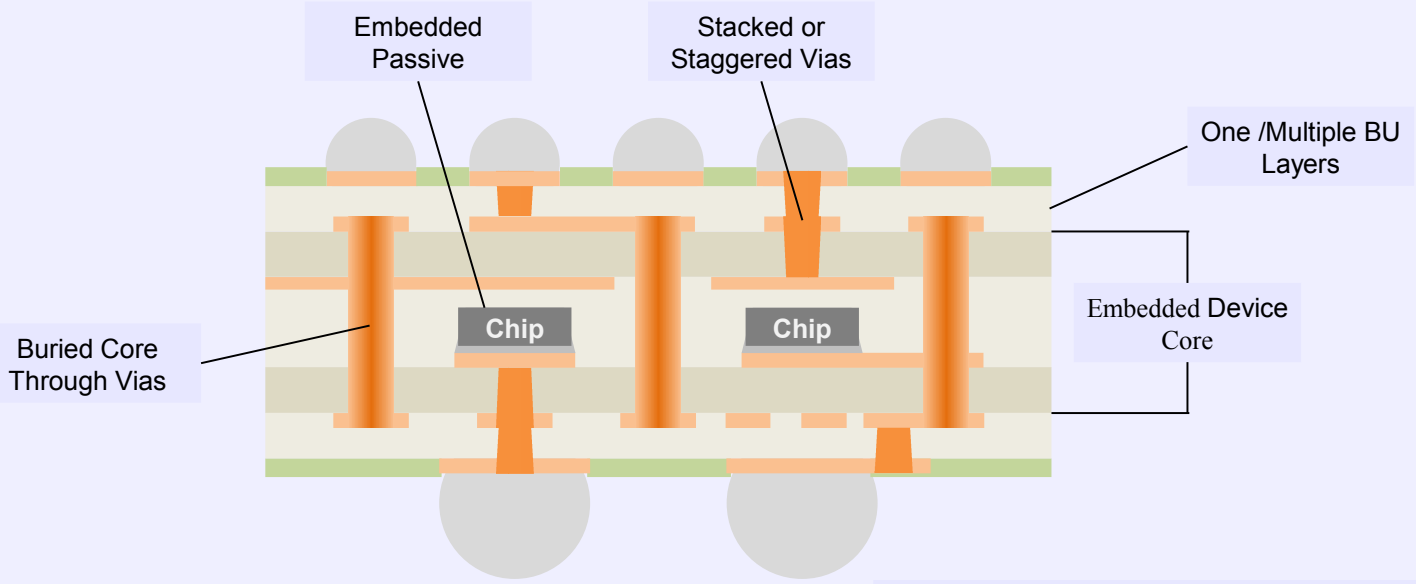
- Vehicles (not demonstrator)
- ICs: back-end processes (F/C on top), stacking
- chip size = 3 different sizes
- Passives: discrettes + IPD
- PoP
- Yield and re-workability
- Module to Board assembly
- Assessment
- Thermal
- RF & EMI
- Reliability
- Specs:
- Supply chain
- KGD

Prop. 1: 3D Embed & WB/FC

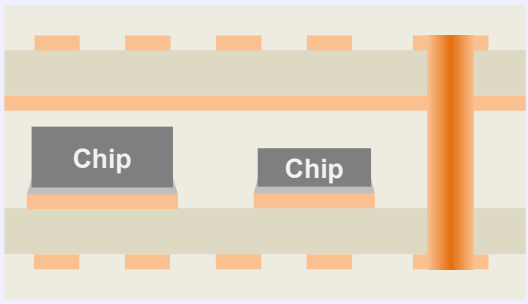


- Each test vehicle consists of unique chip/substrate & package/PCB interconnects
- **Test Vehicle 1 – Improved signal integrity WB/FC comparison package**
 - IC Substrate with embedded discrete passives, capacitors and/or resistors
 - F/C and W/B surface mounted daisy-chain or optional switching chip 12mm x 12mm
 - Design rule simulator
 - Module to board assembly
 - Manufacturing and yield analysis
 - Life-cycle performance/reliability evaluation
 - Provides development path to improve embedded
 - Possible to use common substrate or PCB TVs

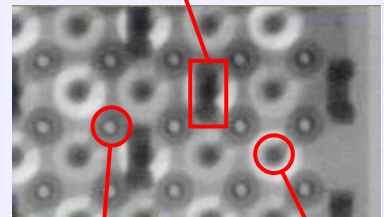
Test Vehicle 1



Multiple Body Size
Option 0201/0402



Embedded decoupling capacitor in core underlying stacked via structure in BU layers

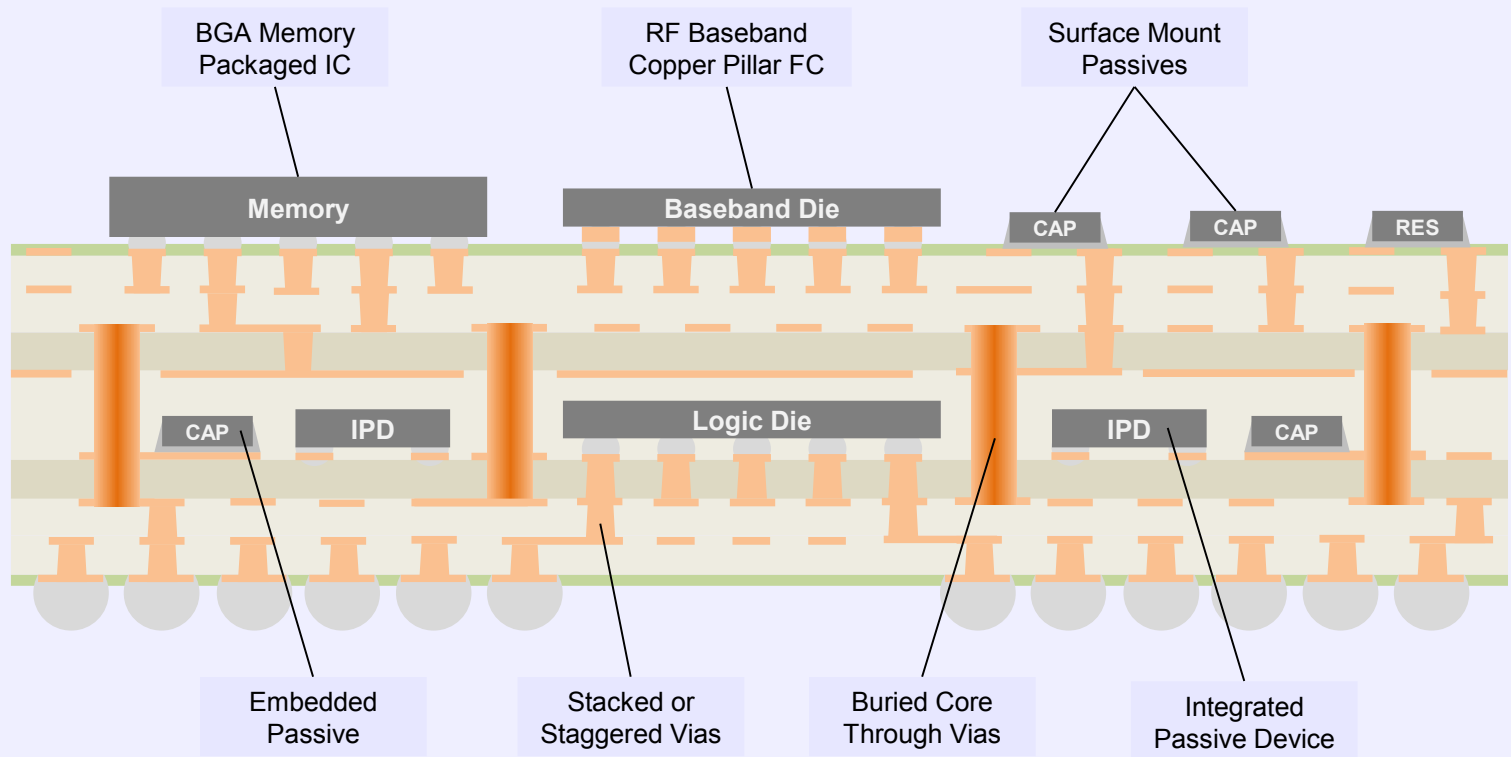


Embedded core IVH connection to devices

Cu filled stacked via connection to BGA

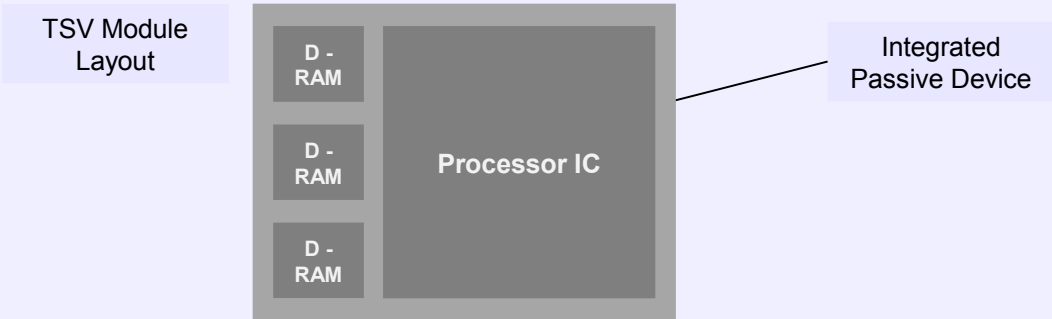
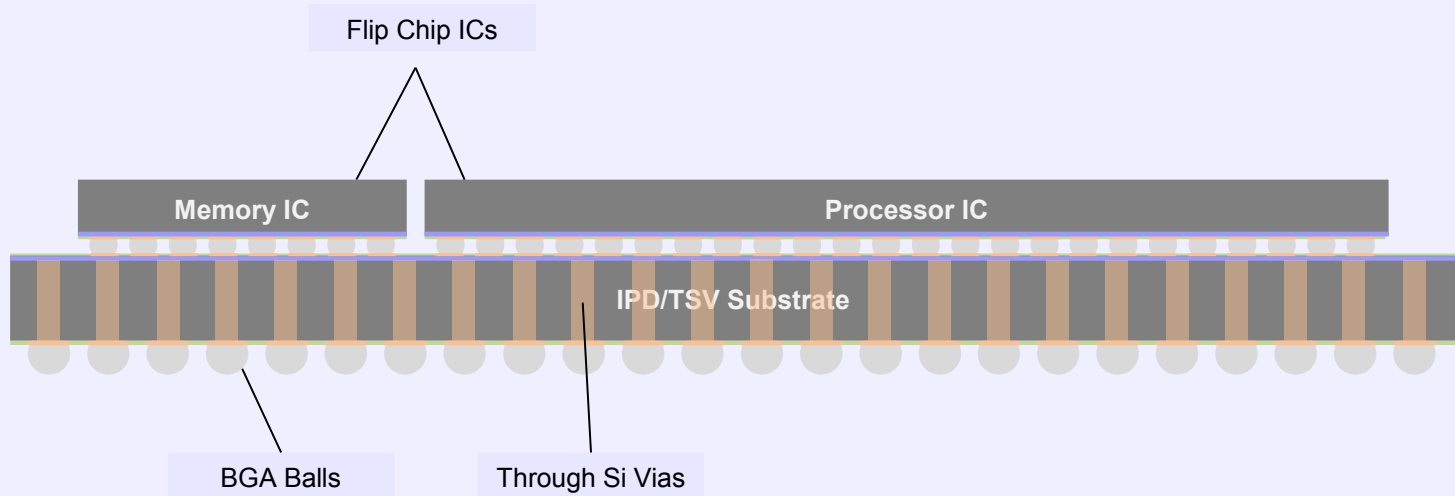
- **Test Vehicle 2 – RF System in Package**
 - Embedded, Flip Chip logic die
 - Flip-Chip, surface mount Baseband Die (on copper pillars)
 - Embedded passives in IPD: Filters, splitters, capacitors
 - Option to include embedded discretes in substrate or PCB if required
 - RF performance including EMI/RFI
 - Module to board assembly
 - Manufacturing and yield analysis
 - Life-cycle performance/reliability evaluation

Test Vehicle 2



- **Test Vehicle 3 – High Speed Switching stacked die package: Thermal performance**
 - Organic or Silicon TSV interposer with flip chip die sites and passive devices (resistors/capacitors)
 - Large (17mm x 17mm or larger) Switching Chip simulator, Flip-Chip Site 1
 - High speed memory chip, Flip-Chip site 2
 - Power generation and temperature measurement in all chips and interposer
 - Thermal structures and thermal performance
 - Module to board assembly
 - Manufacturing and yield analysis
 - Life-cycle performance/reliability evaluation

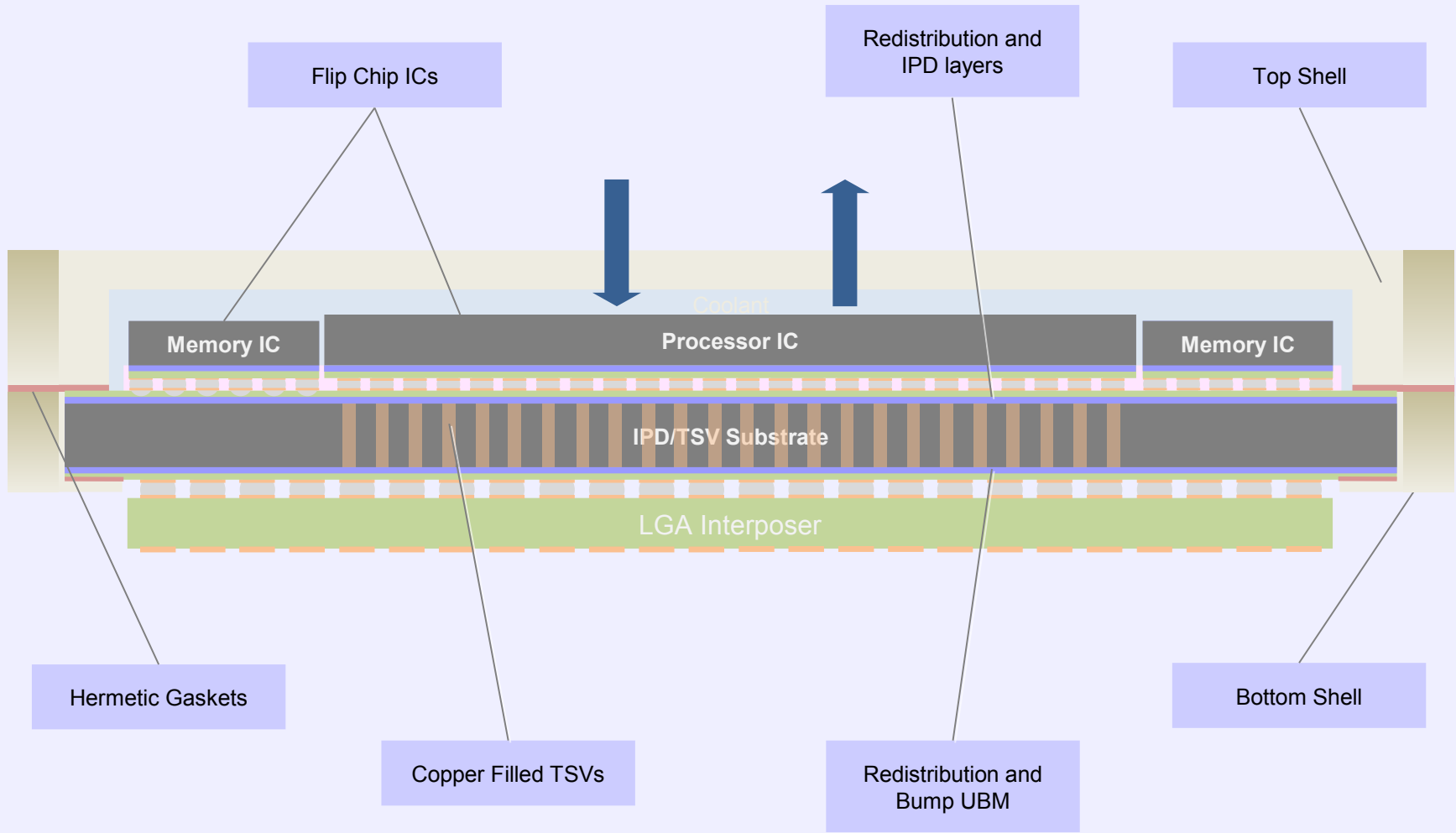
Test Vehicle 3



Proposal 4: TSV & High Density

- **Test Vehicle 4 – High density 3D interconnect**
- Silicon TSV interposer with flip chip die sites: maximize interconnect density
- Embedded and/or surface mount decoupling capacitors (can compare performance)
- 2...4 Large (17mm x 17mm or larger) Switching Chip simulator, Flip-Chip Site
- First design exercise, then build and test if promising
- Manufacturing and yield analysis
- Life-cycle performance/reliability evaluation

Test Vehicle 4



Next steps



- Each potential participant to assess their interest in the 4 proposals with 0 to 5 points
- To elaborate on the most interesting one adding or removing tasks and views.
- To name contact persons for the proposal
- Deadline April 30, 2010