3D + Embedded Device Technology Workshop

High Density Packaging Users Group • Bruchsal • May 18, 2010

Paul Collander, HDPUG, Facilitator
C.B. Katzko, Meadville, Leader

Workshop Agenda

Time	Topic
14:00 – 14:15	Self Introduction
14:15 –14:30	Introduction to 3D Packaging
14:30 – 14:40	Project History
14:40 – 15:00	Member Questionnaire Results
15:00 – 15:45	SiP Module Project Discussion
15:45 – 16:00	Break
16:00 – 16:45	Processor Module Project Discussion
16:45 – 16:50	Communication & Reporting to the HDP Community
16:50 – 17:00	Plan Next Steps
17:00	Conclusion of Meeting

Workshop Agenda

Who's Who in the Workshop

Dave Love, Sun

Dave Towne, Cisco

Hans Juergen Michel, NSN

Deitmar Breisacher, NSN

Martin Schnepf, National Semiconductor

Thomas Nakata, Hitachi

Hiroshi Shimizu, Hitachi

Olivier Gaborieau , IPDIA

Sacha Matic , IPDIA

Rachel Huang, ITRI

Calling In:

Rich Graf, IBM

Po Tse, Phillips

John Martin, Huawei

Kay Essig, ASE

Chris Katzko, Meadville

Paul Collander, HDP Users Group

Marshall Andrews, HDP Users Group

Jack Fischer, HDP Users Group

Rubin Bergman, HDP Users Group

Brian Smith, HDP Users Group

Kim Jorgenson, HDP Users Group

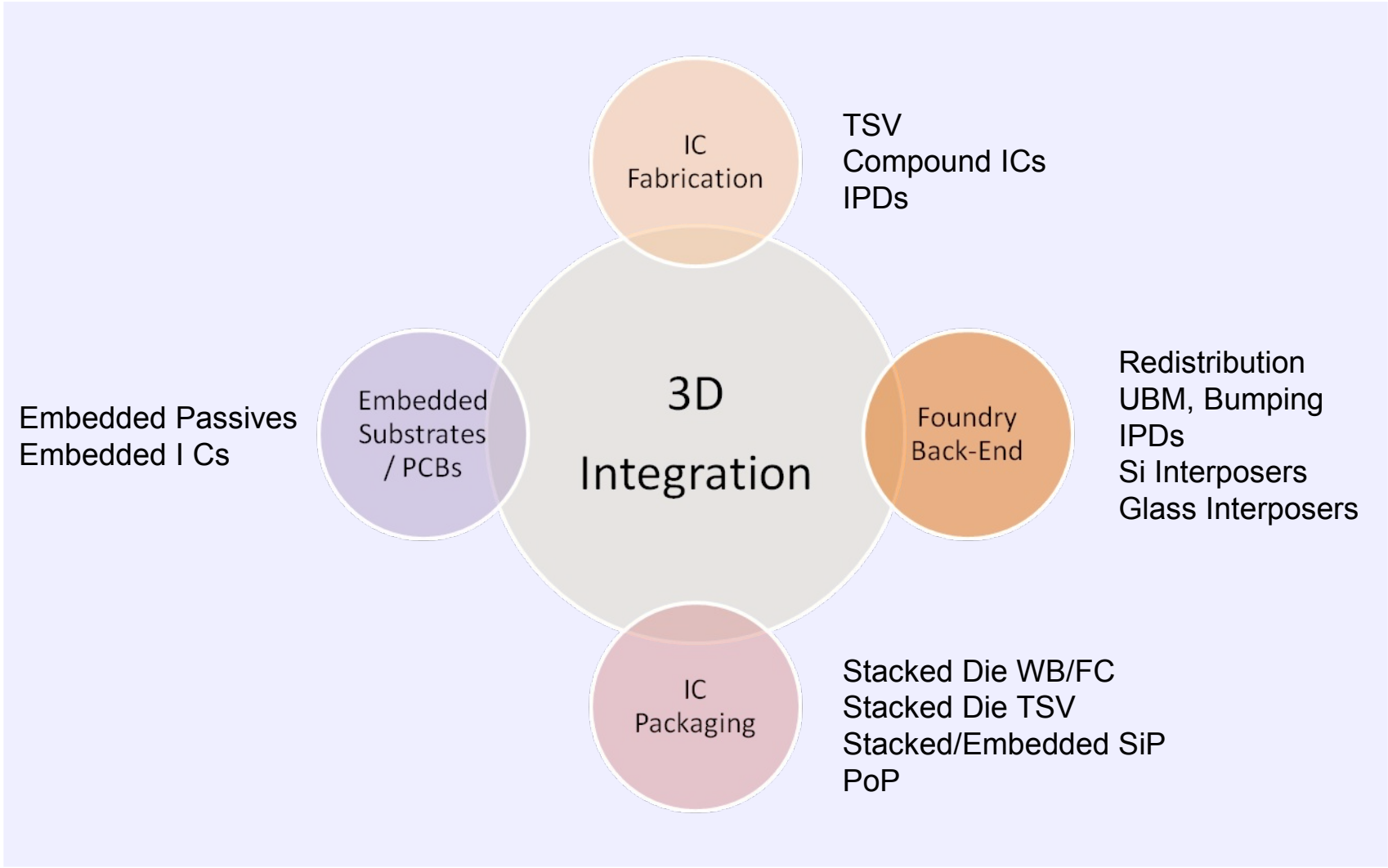
Henry Yang, SYST

Sue Teng, Cisco

Bernd Appelt, ASE

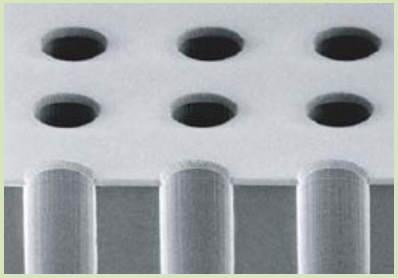
INTRODUCTION TO 3D PACKAGING

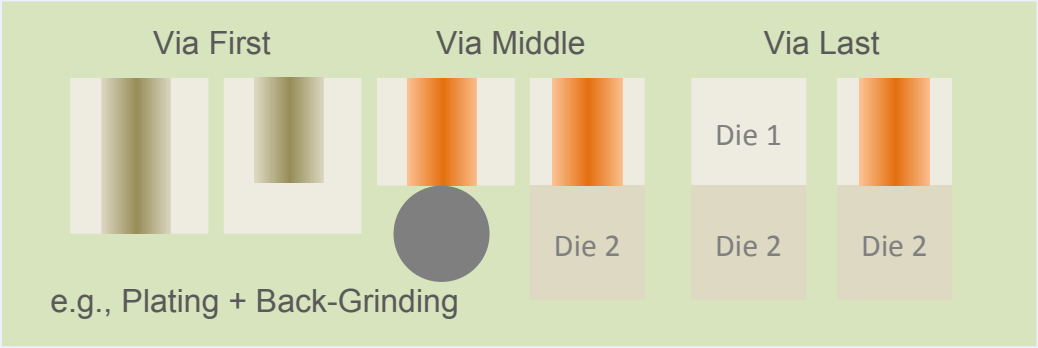
Introduction to 3D



Through Silicon Vias

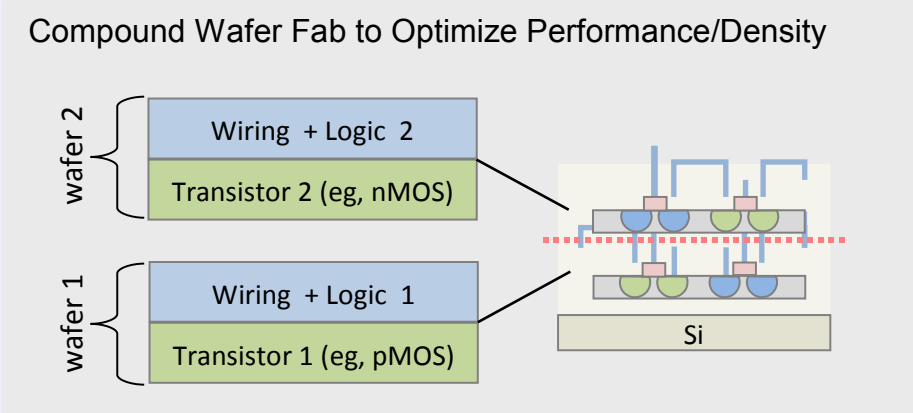
- TSVs extend IC Fab processing to 3D enabling:
  - Die/Die interconnection to fabricate compound ICs
  - Die/Die interconnection of stacked ICs without wire bonding
  - Fabrication of silicon interposers for chip arrays or stacks
  - Formation/integration of thin-film passive devices & interposers
  - Formation of thermal vias and heat dissipation structures
- TSVs evolved from 3D MEMS Fab processes and include:
  - Dry Etch (Deep RIE) formation of cavities, trenches & through vias
  - Laser formation of through vias
  - Back-grinding before or after metallization to create various structures
  - Processing by numerous methods & sequences to create various structures

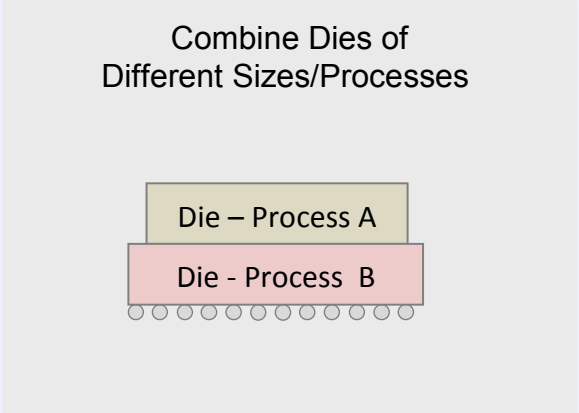




Compound ICs

- Compound ICs manufactured in multiple interactions can create structures that:
  - Combine multiple IC processes, e.g., Si and GAs substrates
  - Create new device architectures
  - Minimize Die/Die interconnects and eliminate stubs from the system
  - Create possibilities for packaging with foundry level processes, precision & design rules
  - Include thermal via structures in the sandwich
- Compound ICs fabricated by back-end processes (after singulation) can:
  - Combine dies of different sizes from different processes
  - Incorporate thin film redistribution circuitry and passive devices (on die or interposer)

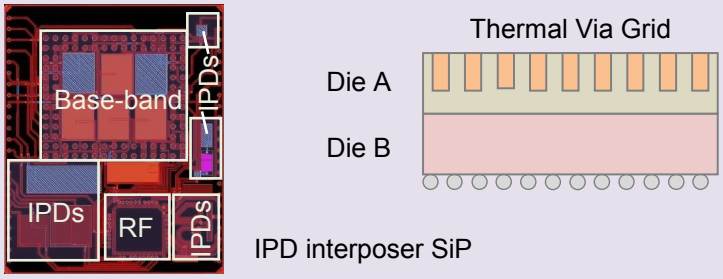




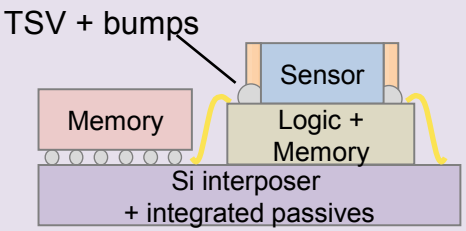
Si Interposers + IPDs

- Si Interposers enable chip-array, chip-stacking systems and SiPs that:
  - Match interposer circuitry design rules and electrical characteristics (thin-film process), achieving high interconnection density
  - Match or minimize CTE differentials for higher reliability/thermal performance
  - Minimize interconnection stub length to reduce parasitics and match impedance
  - Enable integration of passive devices on interposers to improve performance
  - Enable sub-system + SiP on silicon platforms
  - Enable integration of thermal management features, e.g, thermal via arrays
  - Minimize package thickness and area

Integrated Passive Devices + Thermal Management



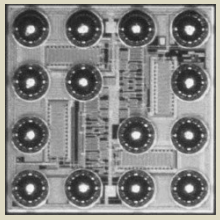
Combine Dies from Different Processes + Create SiPs



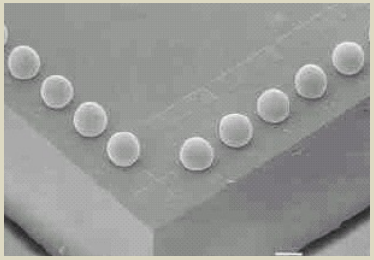
WLCSP + Die Preparation

- Various conventional WLCSP and die preparation technologies enable 3D Ics & SiPs:
  - Passivation, redistribution & bumping
  - UBM & C4 bumping
  - UBM & ACF
  - Au wire stud-bumping & TSB or Compression Joining
  - Laser dicing of peripheral TSVs to form castellations
  - Back-grinding, wafer thinning & annealing
  - C4 & Flip Chip methods

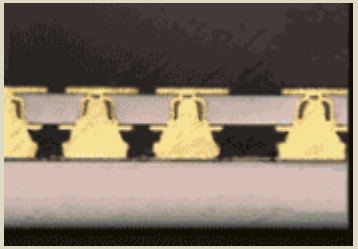
WLCSP process



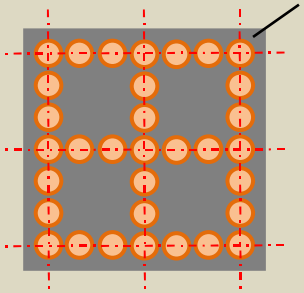
Peripheral Bumping



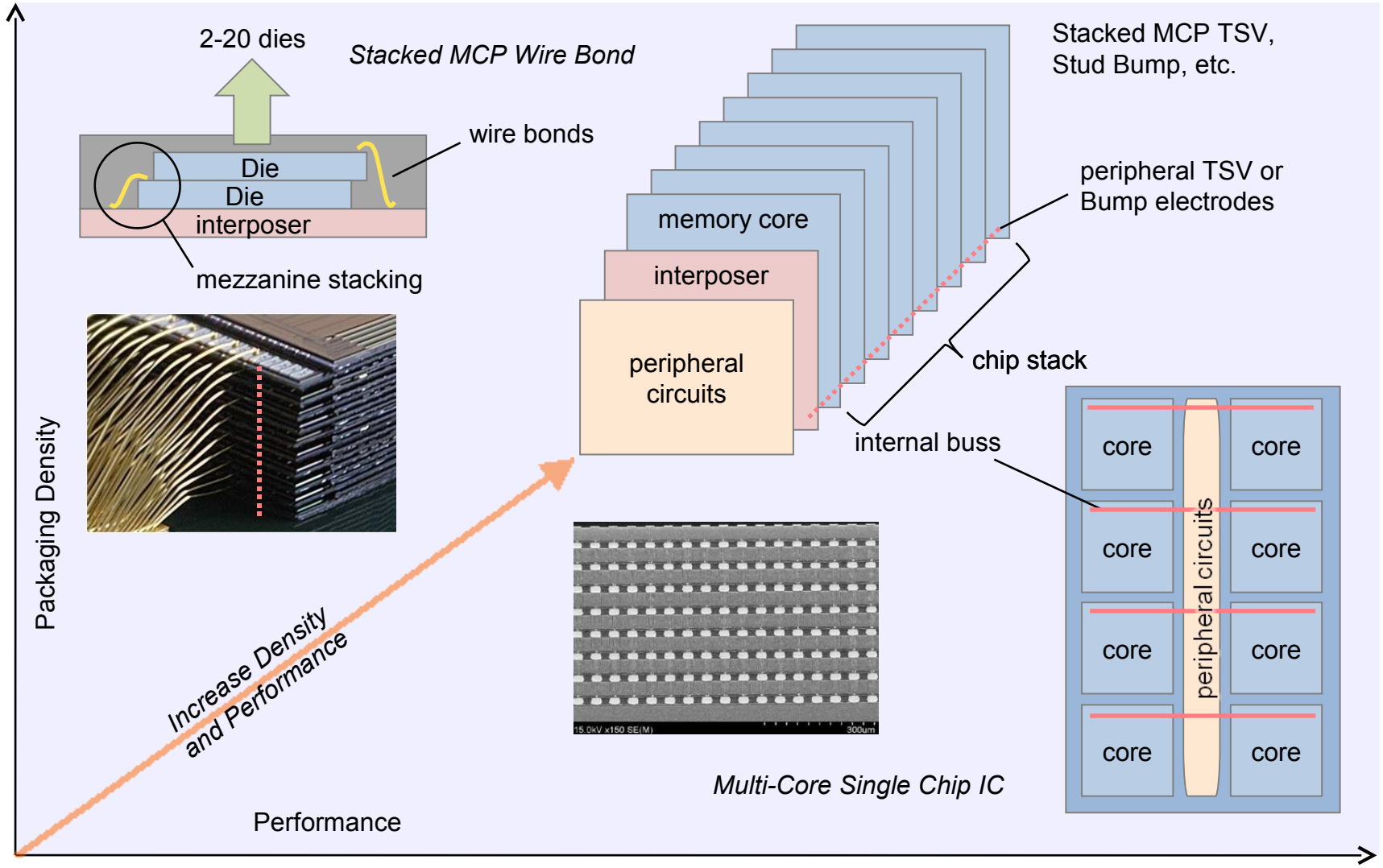
Stud Bumped TSV



Dicing of peripheral vias



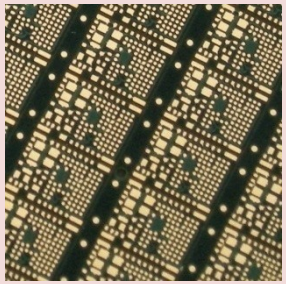
3D Stacked Die IC Packaging



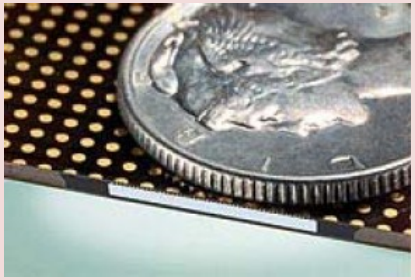
3D Stacked Die IC Packaging

- Stacked Die 3D provides low cost packaging for memory & logic/memory devices
  - Wire Bonded 3D employs conventional interconnection technology where low cost is paramount and wire inductance does not affect performance
  - Peripheral bumped or TSV peripheral bumped die improves performance for high speed memory and wireless applications, e.g., Wifi, Bluetooth, etc.
  - SiP typically employs mixed technologies (WB, FC & SMT passives) and is migrating toward embedded die to eliminate wires and stubs that degrade frequency response
  - Miniaturized CSP modules with 0.40mm or finer BGA are primarily Flip Chip with die bump pitch 160-200um requiring ultra-thin, Via in Pad substrate (e.g. 1+2-+, 2+2+2)

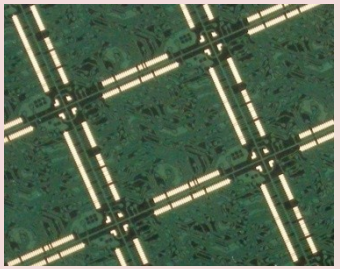
FC + WB Via in Pad
Wireless SiP substrate



Single chip via down
embedded CSP



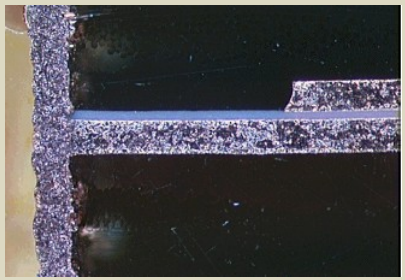
2 Die stacked WB
Substrate



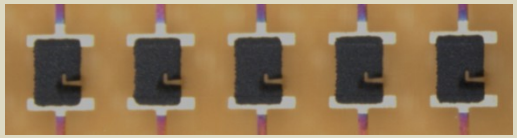
3D IC Substrate & PCB Embedded Devices

- Embedded passives enable performance improvement is IC Packaging (Level 1) and PCB (Level 2) modules:
  - Planar sheet capacitors in PCBs
  - Coil inductors in PCBs including buried/stacked via structures
  - Embedded planer capacitors in IC Substrates
  - Embedded discrete chip capacitors, resistors in IC Substrates and PCB modules in stacked via structures
  - Thin film integrated Passive Devices such as capacitors, chokes, blain transformers and inductors in IC Substrates

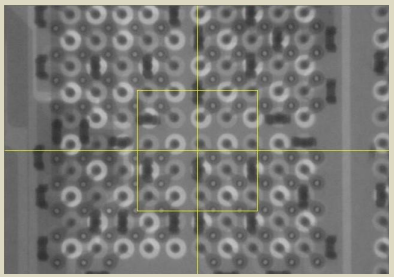
Embedded planer capacitor



Polymer thick film embedded resistor



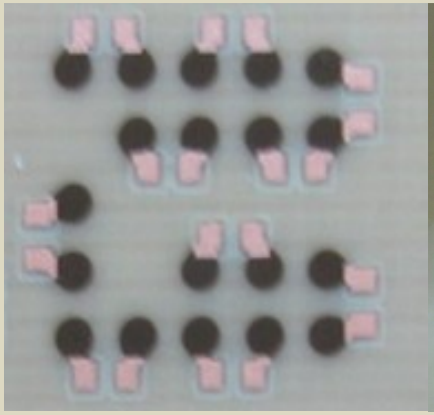
Embedded Discrete Passives 0.8mm BGA



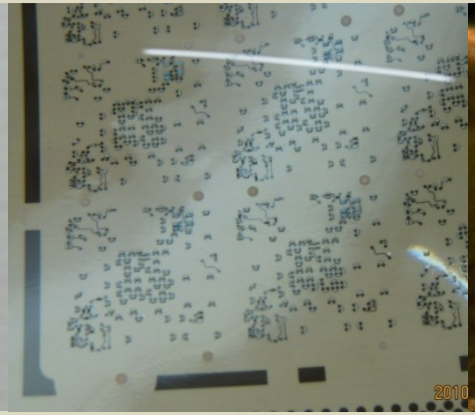
3D IC Substrate & PCB Embedded Devices

- Embedded chip capacitors & resistors:
  - 0201 low profile devices are preferable to minimize thickness
  - Generally embedded on one layer in center core to minimize thickness and warpage
  - Can be embedded on any build-up layer
  - Lead Free assembly

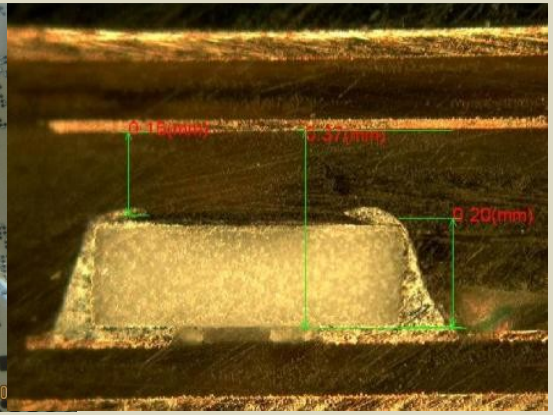
Masked Pads Prior to Assembly



Sub-Assembly



Embedded Capacitor in 0.7mm pitch PBGA



PROJECT HISTORY

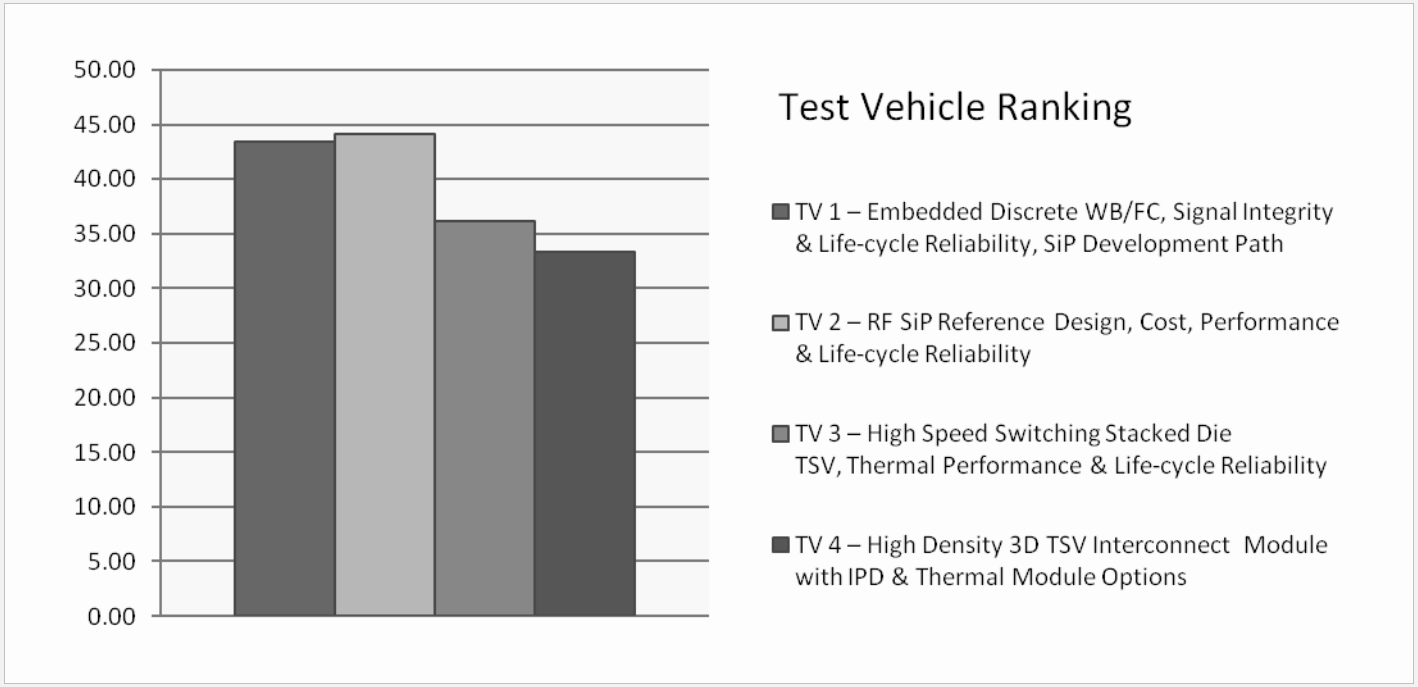
Project History

- Project concept developed in 2009 as spin-off of WiMax SiP
- Preliminary member survey Dec/Jan 2010 reported in March 2010 meeting
- Ad hoc working group developed 4 test vehicle proposals Mar/April 2010
- Membership questionnaire April 2010

- Current proposals
- TV 1 & TV2 embedded move to proposal stage
- TV3 & TV4 need additional discussion with stakeholders to refine concepts

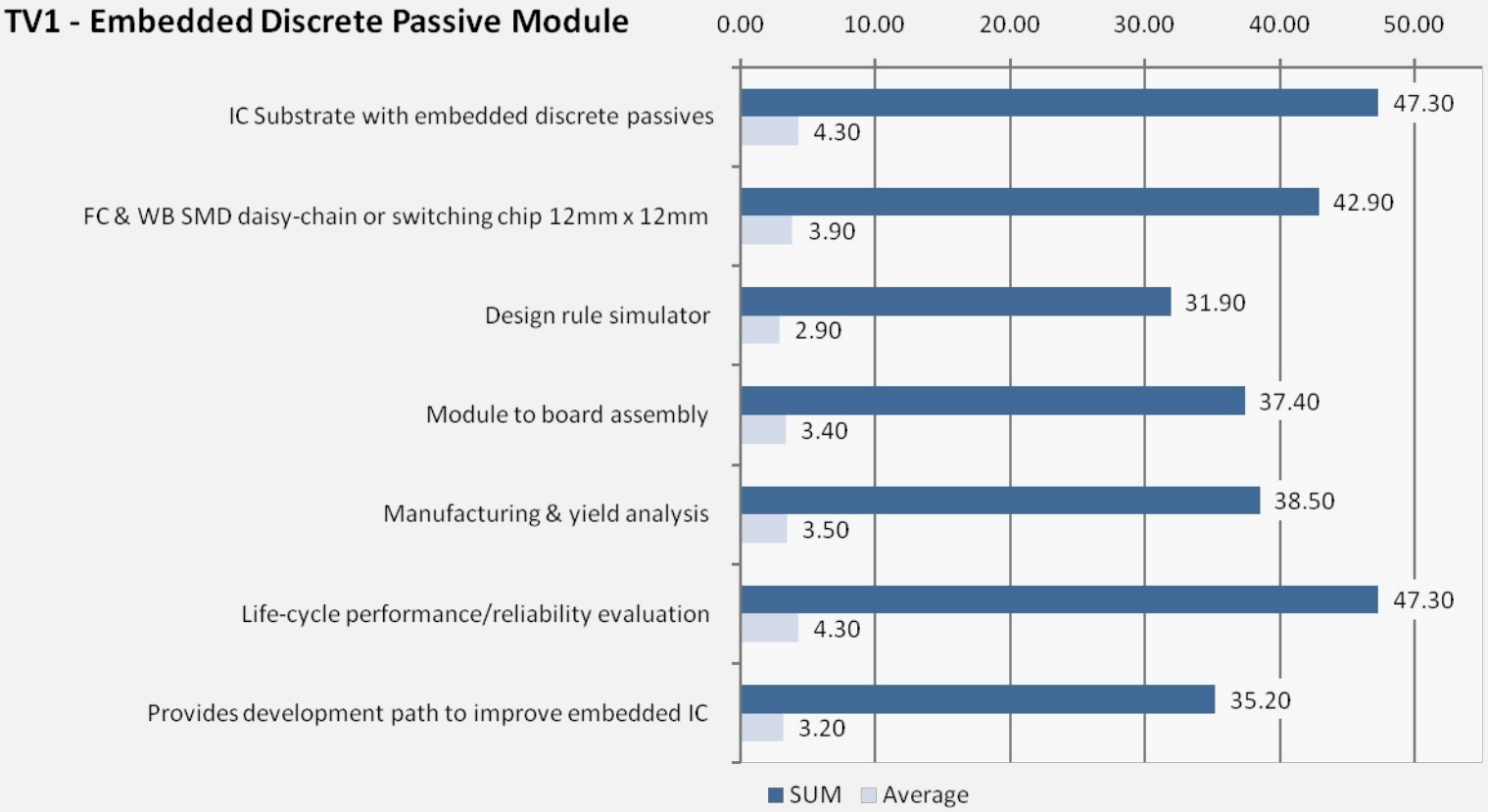
MEMBER QUESTIONNAIRE RESULTS

Member Questionnaire Results

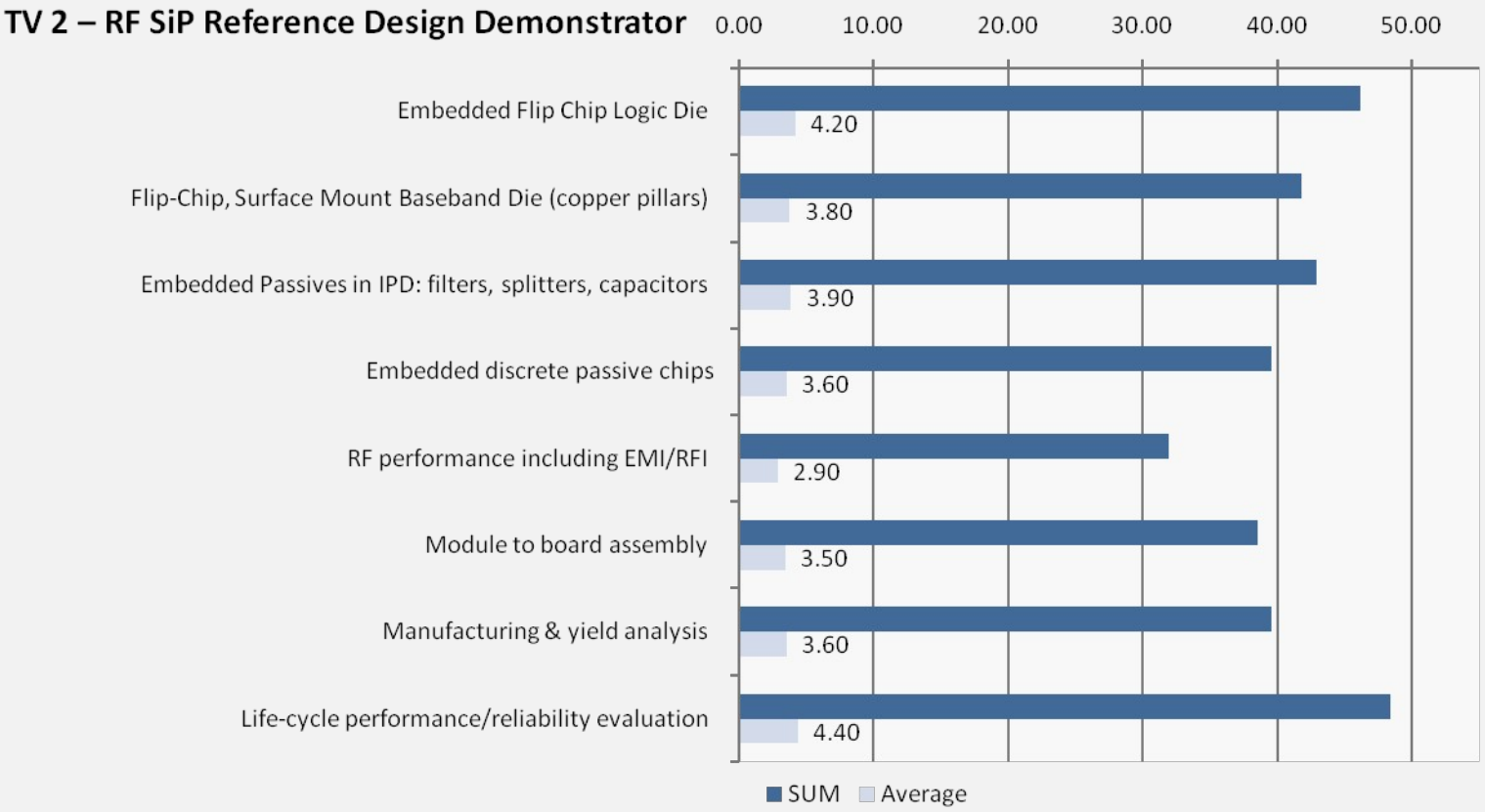


- Propose to divide the project into 2 modules by basic technology:
  - Embedded substrate TV1 & TV2 (or direct to TV2)
  - Stacked Die TSV ICs/Interposers TV3 followed by TV4

Member Questionnaire Results

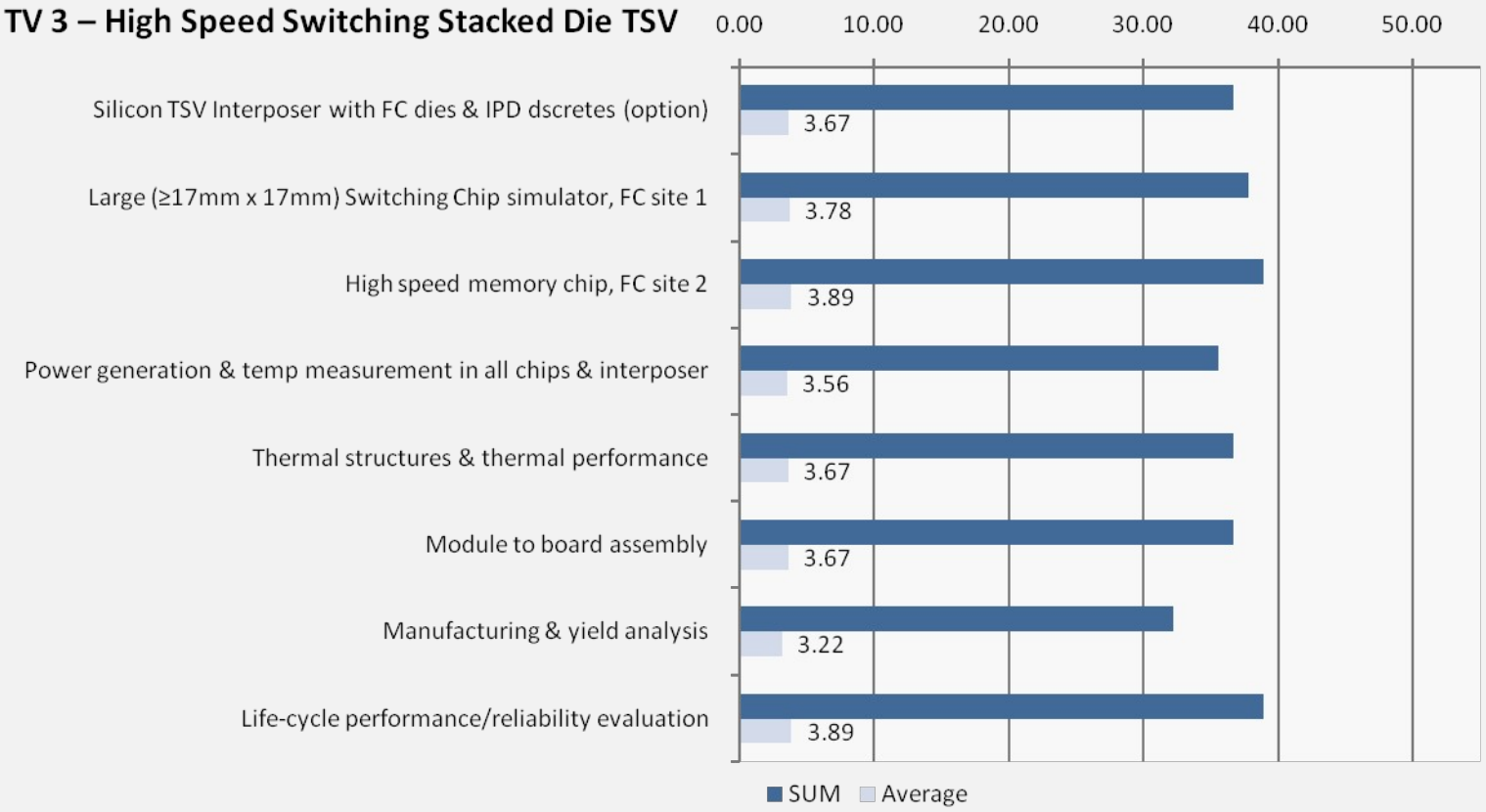


Member Questionnaire Results



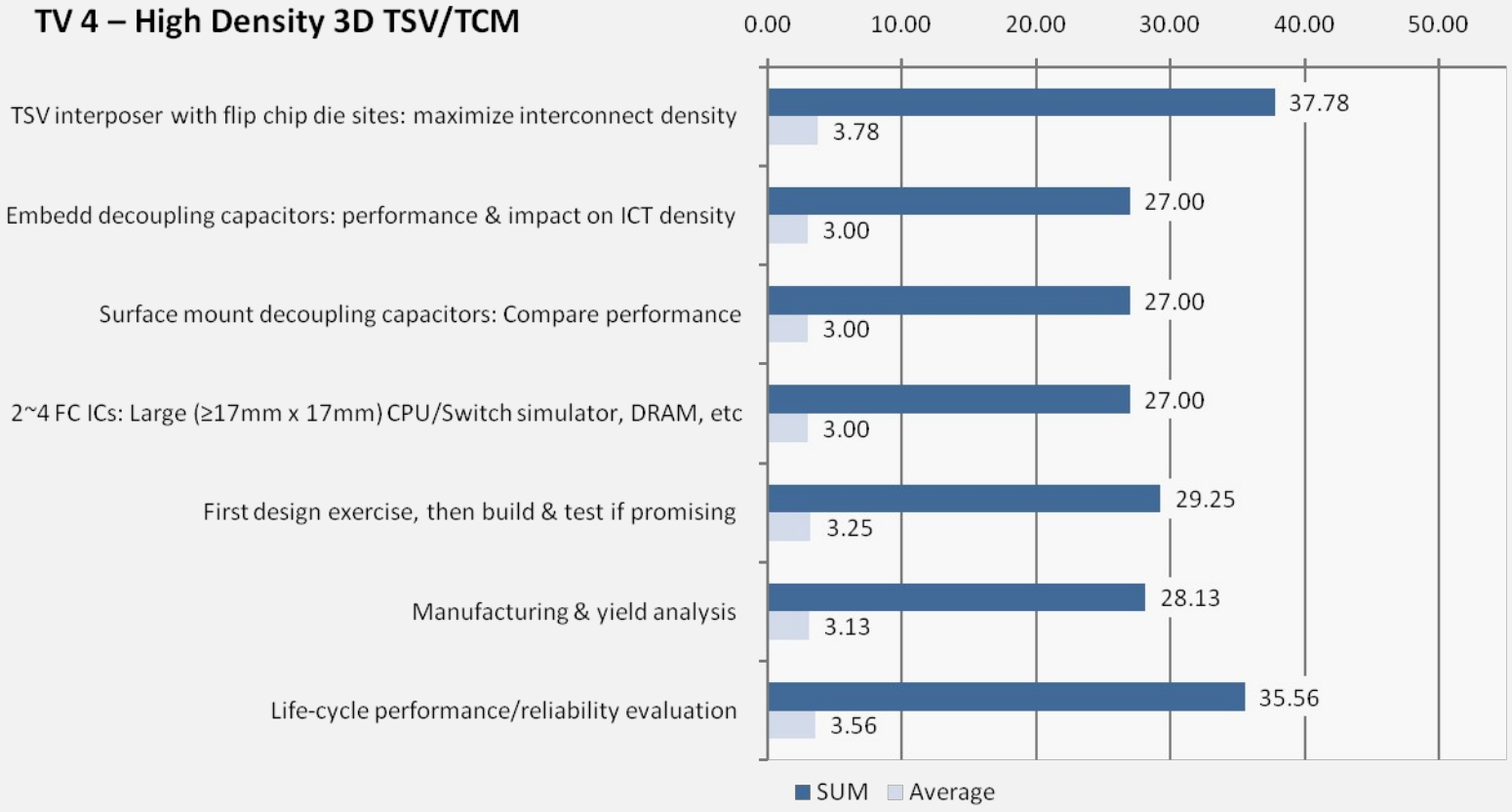
- Cost Analysis is an additional high interest item

Member Questionnaire Results



- Thermal Analysis is a critical concern, on-die sensors needed

Member Questionnaire Results

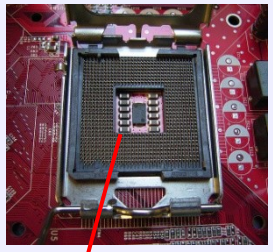


- Requires application-specific design development

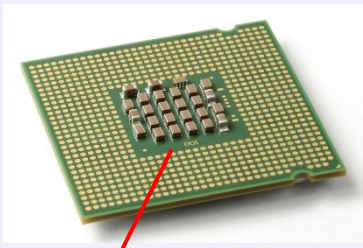
SINGLE CHIP MODULE/SIP MODULE PLANNING

TV1 - 3D Embedded Passives

- Test Vehicle 1 demonstrates single chip package systems applications where embedded passive devices are used to improve signal integrity & performance
- Test structures to be compared could include:
  - Switching IC in Flip Chip surface mount (performance baseline)
  - Optional switching IC in Wire Bond surface mount (to compare FC/WB)
  - Various decoupling capacitor structures connecting to the IC's:
    - SMT chip capacitors remotely mounted on substrate module or PCB
    - SMT chip capacitors mounted on bottom of substrate opposite IC
    - Embedded chip capacitors within BGA grid with direct connection to IC
    - Embedded IPC capacitors to compare performance to ceramic capacitors
- Test vehicle consists of:
  - Switching ICs with thermo sensors on die
  - Ceramic chip & IPD (option) capacitors
  - Organic multilayer substrates
  - Printed Circuit Boards

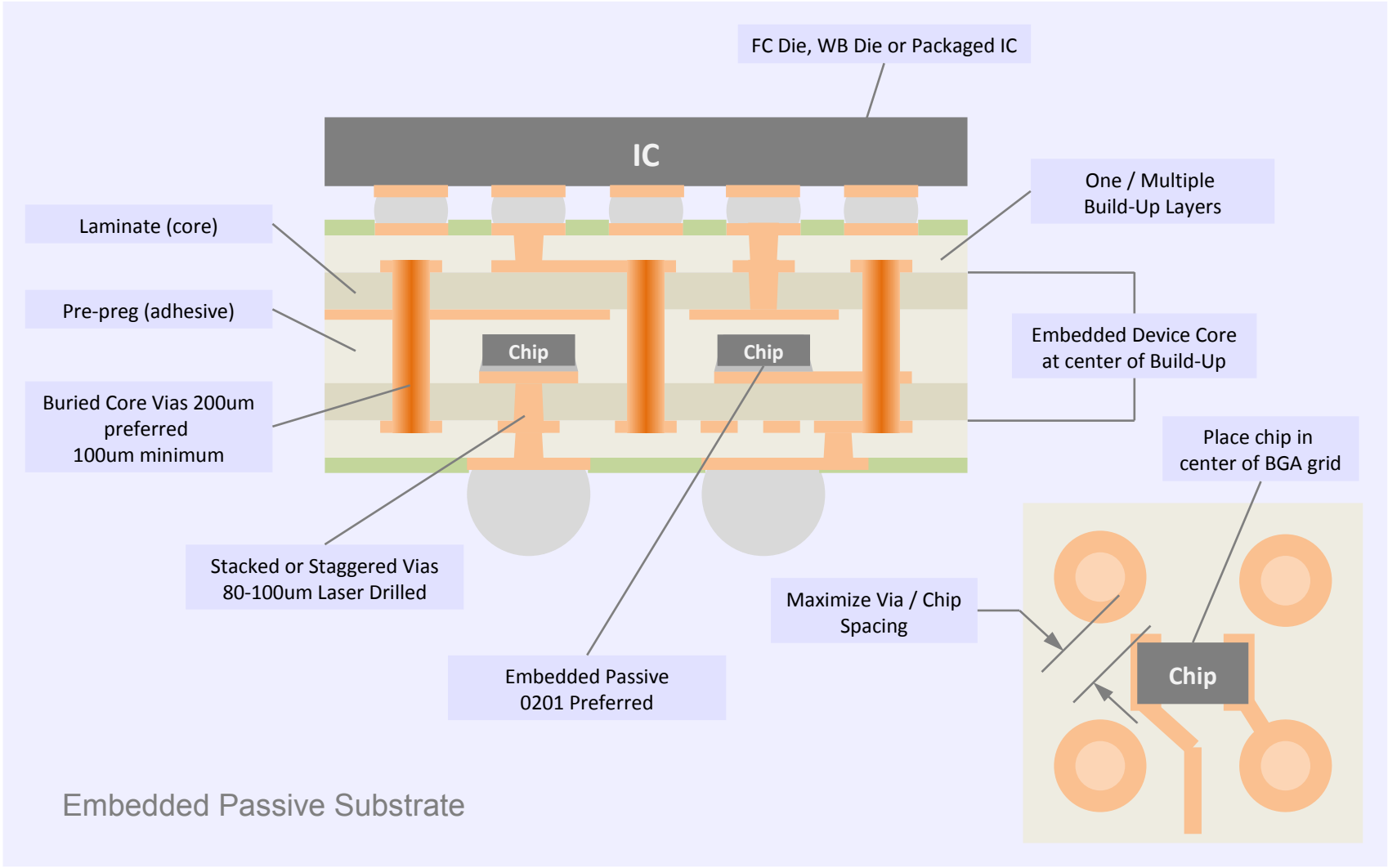


PCB mounted caps



Substrate mounted caps (opposite IC)

TV1 - Embedded Passive Module Concept



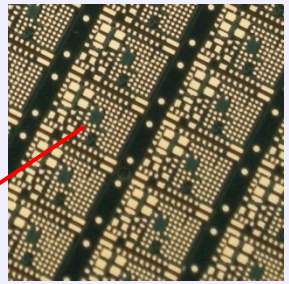
TV1 - 3D Embedded Passive

- Test metrics include:
  - Manufacturing Yield (infant mortality) through ICT
  - Electrical performance comparison
  - Thermal performance comparison
  - Reliability through at least 2000 cycles or failure
  - Failure analysis and root cause assignment
- Resource commitments
  - IC's (sponsor needed)
  - Chip passives – low profile 0201 caps (sponsor needed)
  - IPD passives (sponsor needed)
  - Substrates & PCBs (Meadville TTM, can include passives if needed)
  - Package assembly & test (sponsor needed)
  - Board Assembly & test (sponsor needed)
  - Reliability testing (sponsor needed)
  - Failure analysis (sponsor needed)

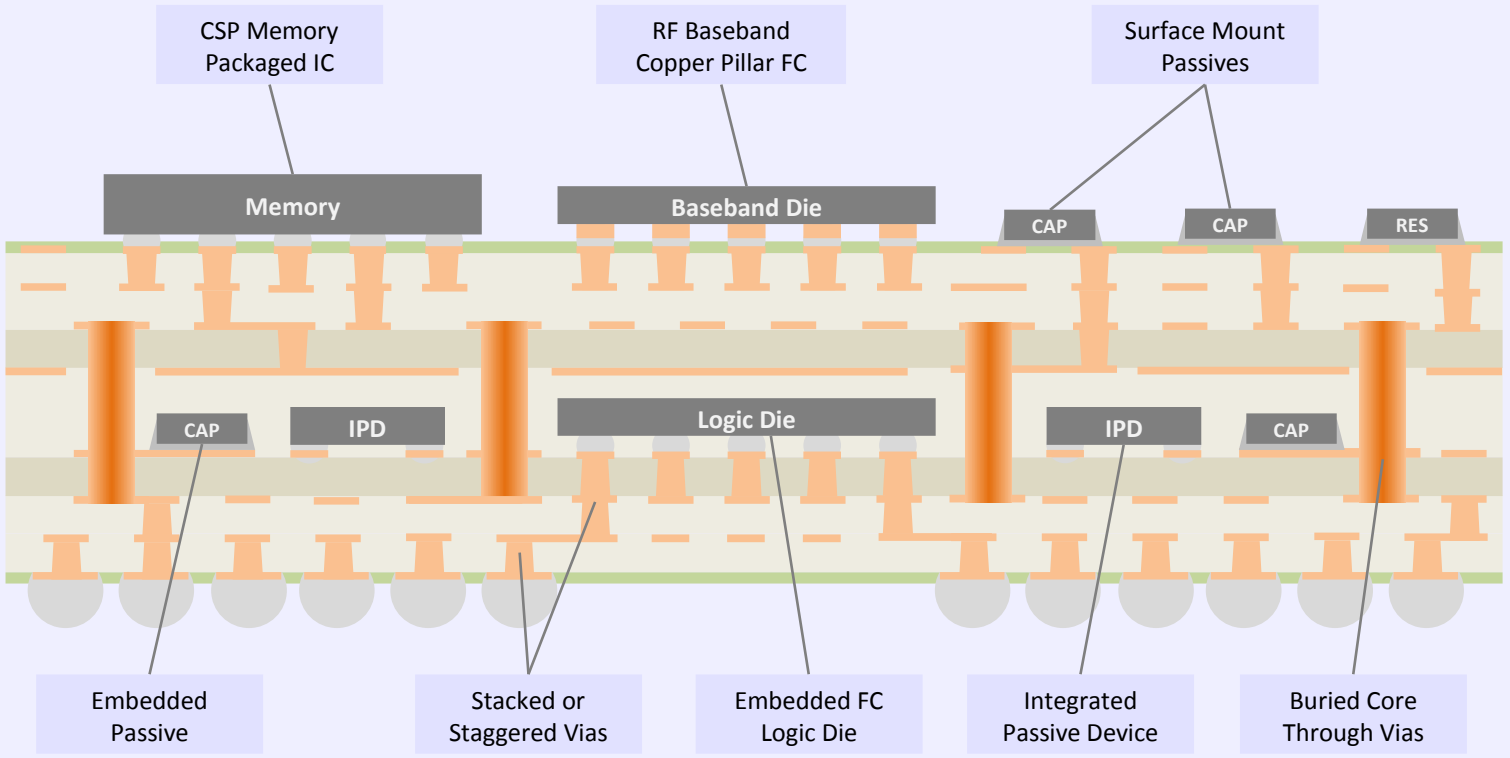
TV2 - 3D Embedded IC RF SiP

- Test Vehicle 2 demonstrates a multiple chip RF SiP application where embedded passives & ICs are used to improve performance, miniaturize & reduce overall cost
- Demonstrator requires a reference design WiFi, Bluetooth or equivalent RF design and could include the following target features:
  - Embedded FC logic IC, preferably with thermo sensors on die
  - Surface mount, copper pillar FC baseband IC, with thermo sensors on die
  - Memory as bare die or package
  - Ceramic chip & IPD passive devices as required (may include capacitors resistors, filters, chokes, etc)
  - Organic multilayer substrates with embedded devices
  - Printed Circuit Boards
- Ideally, the reference design would have been characterized as a surface mount SiP for comparison purposes

Substrate for conventional FC/SMT RF SiP



TV2 - RF SiP Demonstrator Concept



RF SiP Embedded Die Package

TV2 - 3D Embedded IC RF SiP

- Test metrics include:
  - Manufacturing Yield (infant mortality) through ICT
  - Electrical, RF & EMI/RFI performance
  - Thermal performance
  - Reliability through at least 2000 cycles or failure
  - Failure analysis and root cause assignment
- Resource commitments
  - Reference design (sponsor needed)
  - IC chip sets (sponsor needed)
  - Chip passives, various types as required (sponsor needed)
  - IPD passives, various types (sponsor needed)
  - Substrates & PCBs (Meadville TTM, may need FC assy for embedded IC)
  - Package assembly & test (sponsor needed)
  - Board Assembly & test (sponsor needed)
  - Reliability testing (sponsor needed)
  - Failure analysis (sponsor needed)

SiP Module Tasks

Tasks	Scheduled	Actual
Plan Project		
Board design and verification		
Approval by project members		
All components received		
Fabricate and electrically test packages & PCBs		
Prepare wiring for Data Acquisition System		
Assemble & inspect boards		
Data Acquisition wiring soldered to all boards (prep for test)		
Start Thermal Cycle (ATC) Tests		
Run Shock & Vibration and/or Performance Tests		
Stop ATC Tests		
Start Failure Analysis		
Complete Failure Analysis		
Complete Project Report		
Publish report to HDP Membership		

15 Minutes, Please!

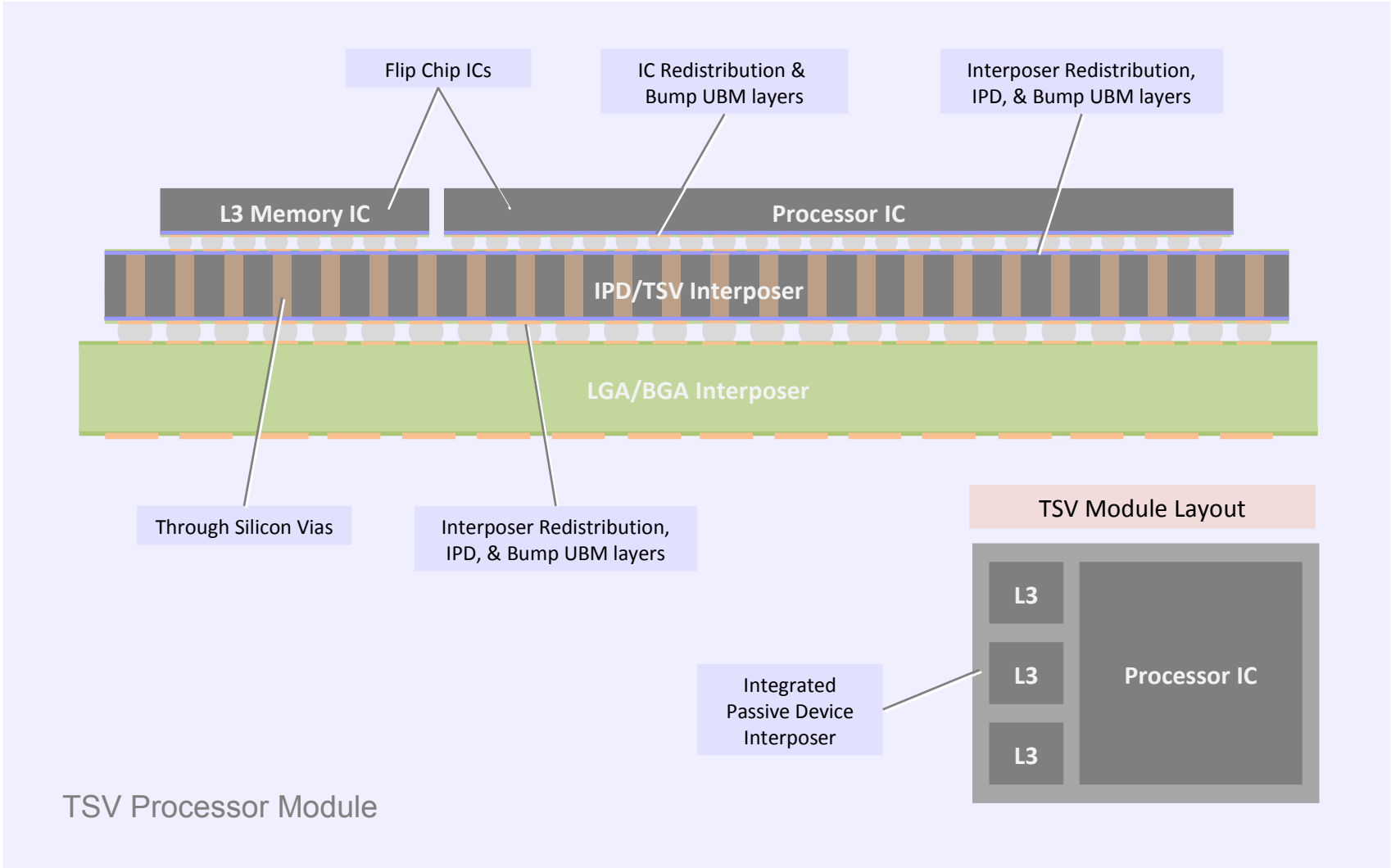
COFFEE BREAK

PROCESSOR MODULE PLANNING

TV3 – TSV Interposer Processor Module

- TV3 demonstrates a high performance switching processor with L3 memory Flip Chip mounted on a TSV interposer with redistribution/logic circuits and IPBs on an organic LGA/BGA substrate
- Demonstrator requires:
  - Switching chips ≥17x17mm with thermo sensors on die (sponsor needed)
  - High speed L3 memory dies (sponsor needed)
  - A custom TSV interposer with IPD
  - Organic multilayer LGA/BGA substrate with embedded passives if required (Meadville/TTM)
  - Printed Circuit Boards with LGA sockets if required (Meadville/TTM)
  - Support for C4 stacked die assembly on TSV interposer (sponsor needed)
  - Support for Package & Test, PCB assembly/test (sponsor needed)
  - Failure Analysis support (sponsor needed)

TV3 - Processor Module Concept



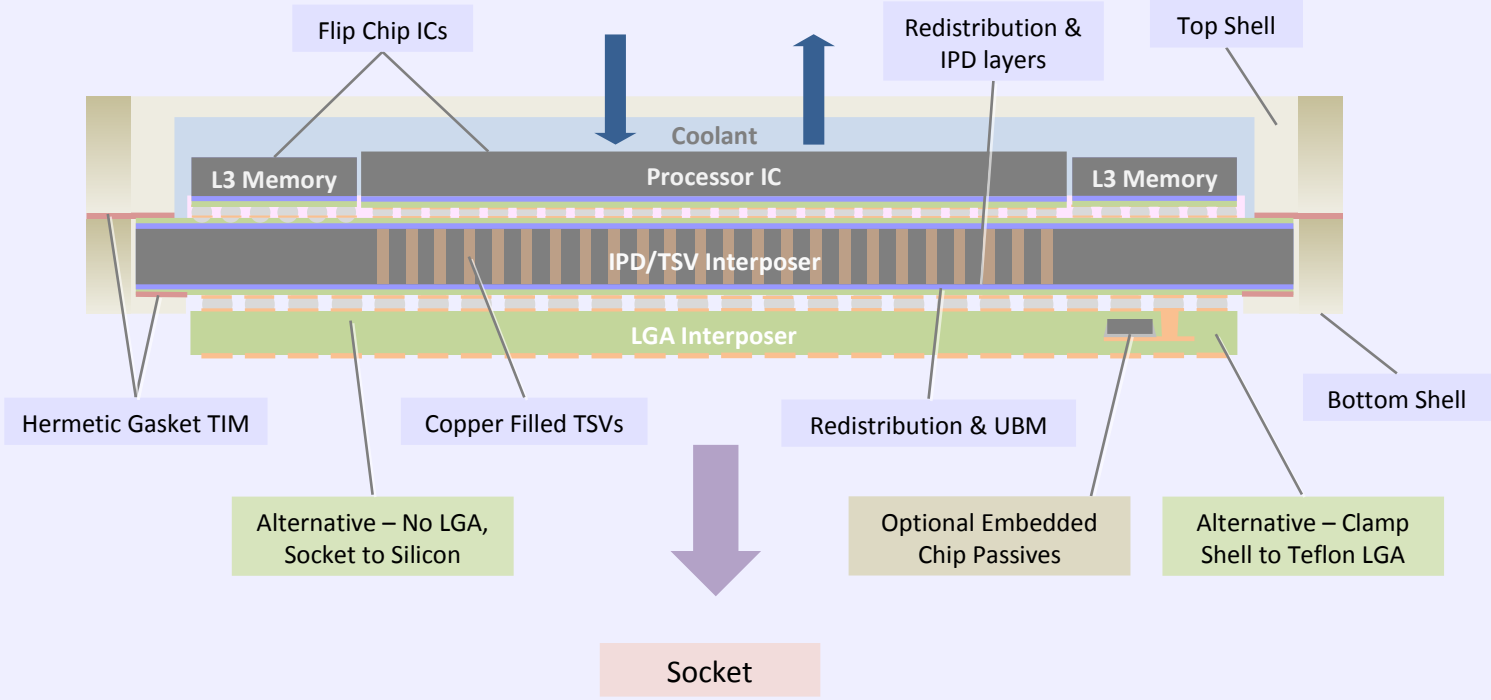
TV1 - 3D Embedded Passive

- Test metrics include:
  - Manufacturing Yield (infant mortality) through ICT
  - Electrical performance comparison
  - Thermal performance comparison (critical item)
  - Reliability through at least 2000 cycles or failure
  - Failure analysis and root cause assignment
- Resource commitments
  - IC's (sponsor needed)
  - Chip passives – low profile 0201 caps (sponsor needed)
  - IPD passives (sponsor needed)
  - Substrates & PCBs (Meadville TTM, can include passives if needed)
  - Package assembly & test (sponsor needed)
  - Board Assembly & test (sponsor needed)
  - Reliability testing (sponsor needed)
  - Failure analysis (sponsor needed)

TV4 – TSV Interposer Thermal Control Module

- TV4 demonstrates a high performance switching processor with L3 memory Flip Chip mounted on a TSV interposer with redistribution/logic circuits and IPBs contained within a liquid convection module with or without organic LGA/BGA substrate (PTFE laminate if contained in the hermetic structure)
- Demonstrator requires:
  - Switching chips ≥17x17mm with thermo sensors on die (sponsor needed)
  - High speed L3 memory dies (sponsor needed)
  - A custom TSV interposer with IPDs and copper filled TSVs (sponsor needed)
  - Thermal Control Module & coolant circulation system (Sponsor needed)
  - Organic multilayer LGA/BGA substrate with embedded passives if required (Meadville/TTM)
  - Printed Circuit Boards with LGA sockets if required (Meadville/TTM)
  - Support for C4 stacked die assembly on TSV interposer (sponsor needed)
  - Support for Package & Test, PCB assembly/test (sponsor needed)
  - Failure Analysis support (sponsor needed)

Thermal Module Demonstrator Concept



IPD Interposer & Stacked IC Array Thermal Module

TV4 – TSV Interposer Thermal Control Module

- Test metrics include:
  - Manufacturing Yield (infant mortality) through ICT
  - Electrical performance comparison
  - Thermal performance comparison (critical item)
  - Reliability through at least 2000 cycles or failure
  - Failure analysis and root cause assignment
- Resource commitments
  - IC's (sponsor needed)
  - Chip passives – low profile 0201 caps (sponsor needed)
  - IPD passives (sponsor needed)
  - Substrates & PCBs (Meadville TTM, can include passives if needed)
  - Package assembly & test (sponsor needed)
  - Board Assembly & test (sponsor needed)
  - Reliability testing (sponsor needed)
  - Failure analysis (sponsor needed)

Processor Module Tasks

Tasks	Scheduled	Actual
Plan Project		
Board design and verification		
Approval by project members		
All components received		
Fabricate and electrically test packages & PCBs		
Prepare wiring for Data Acquisition System		
Assemble & inspect boards		
Data Acquisition wiring soldered to all boards (prep for test)		
Start Thermal Cycle (ATC) Tests		
Run Shock & Vibration and/or Performance Tests		
Stop ATC Tests		
Start Failure Analysis		
Complete Failure Analysis		
Complete Project Report		
Publish report to HDP Membership		

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Thank You !

Questions? Comments?

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