Advanced QFN Project

Project leader: Li Li (lili2@cisco.com)
Facilitator: Brian Smith (brians@hdpug.org)

Background

- Quad flat no-lead (QFN) package has been used widely since its introduction in 1998.
- The board design-related issues are critical to understand when QFN pad pitch is 0.4 mm or smaller and the number of package pad rows is 2 or more.
- This project will bridge QFN package suppliers, contract manufacturers, and their customers to improve assembly yields and solder joint reliability together. Package suppliers will work in this project with their material suppliers

Objective

- Enable robust design of QFN package.
- Optimize PCB and its solder pad designs to ensure high board assembly yield on all pins and central pads.
- Ensure robust package & solder joint reliability.
- Promote QFN technology innovation.

Challenges

- Evolution of QFN packaging technology
  - Body size increase
  - Pitch reduction
  - Introduction of multi-row I/O
  - Chip-on-Lead (COL)
  - Top exposed pad (TEP)
  - Power option with solder die attach
  - Multi chip module (MCM) application
- Assembly Process
  - Pb-free and rework process requirements
- Quality and Reliability requirements

Project Goals

- Conduct QFN technology roadmap and supply chain capability survey
- Optimize PCB designs and develop the Design for Manufacturing (DFM) best practice guidelines for QFN
- Engage component suppliers and EMS providers on optimizing package / board designs to maximize board assembly, yield and solder joint reliability
- Establish board assembly and rework processes and best practice
- Assess QFN board level reliability with a test vehicle including selected QFN packages and PCB pad designs for volume assembly/testing and yield optimization

Major Tasks

- Conduct QFN technology roadmap and supply chain capability survey
- Collection of assembly issues identified
- Develop board & stencil design, metallurgical variables, including HDPUG experience of Pb-free metallurgies to suggest improvements
- Design, produce and assemble a test board for daisy chain QFNs
- Perform environmental tests according to HDP practices
- Perform FA and identify weak points to be addressed in a follow-up project

Focused Areas – DOE Parameters

QFN Package:

- Body size, I/O count, pitch, # of rows, die to package ratio, lead finish

PCB Designs:

- Pad-stack designs for both I/O and exposed die pads

Assembly Process Development

- **Pb-free** assembly process
- Stencil designs & selection
- Solder paste selection
- Rework process development

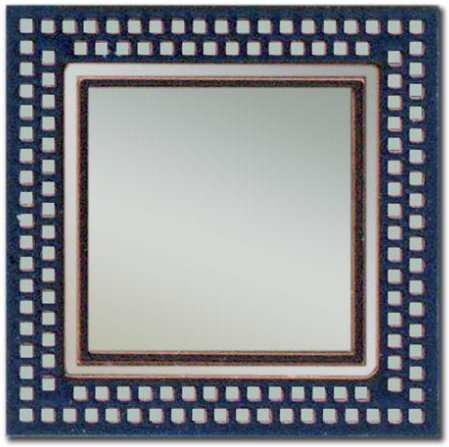
Test Vehicles

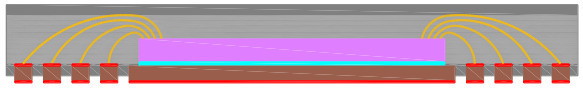
- Test Components
- Test Board Design
  - Layout
  - Board Material
  - Board Layer Stack Up

Test Components

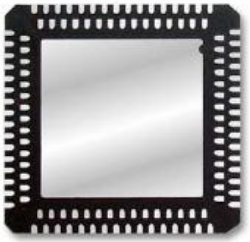
QFN Package:

- Body size, I/O count, pitch, # of rows, die to package ratio, lead finish





XSON6



Outer Leads

Inner Leads

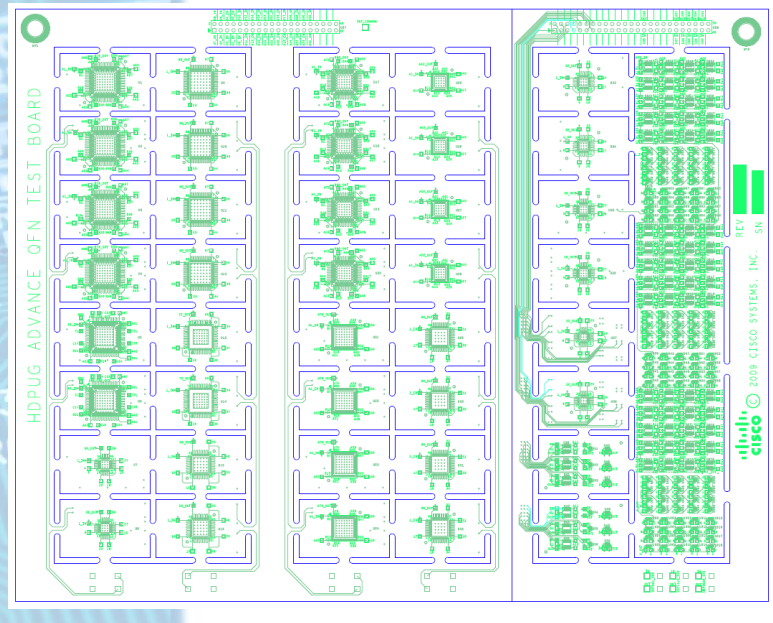
(Source: Amkor, ASAT & NXP)

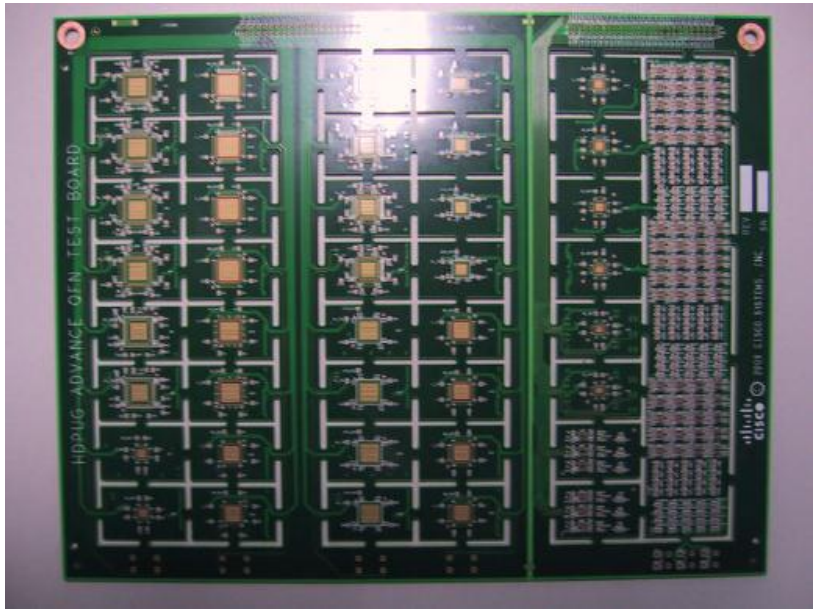
Test Components Selected

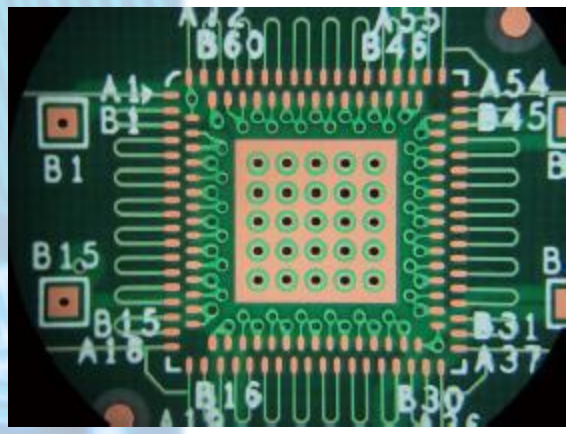
QFN Body Size (mm x mm)	Die Size (mm x mm)	Lead Pitch (mm)	Lead Count	Height (mm)	Number of I/O Pad Rows	Lead Finish	Exposed Die Paddle (mm x mm)	Supplier	Delivery Schedule
5 x 5	3 x 3	0.5	32	0.85	1	Matte Sn	3.5 x 3.5	Amkor	Delivered
8 x 8	5 x 5	0.5	56	0.85	1	Matte Sn	6.1 x 6.1	Amkor	Delivered
10 x 10	7 x 7	0.5	72	0.85	1	Matte Sn	7.5 x 7.5	Amkor	Delivered
5 x 5	3 x 3	0.4	36	0.85	1	Matte Sn	3.7 x 3.7	Amkor	Delivered
8 x 8	5 x 5	0.4	68	0.85	1	Matte Sn	6.5 x 6.5	Amkor	Delivered
10 x 10	7 x 7	0.4	88	0.85	1	Matte Sn	8.1 x 8.1	Amkor	Delivered
5 x 5	3 x 3	0.4	36	0.85	1	NiPdAu	3.5 x 3.5	Amkor	Delivered
8 x 8	5 x 5	0.4	68	0.85	1	NiPdAu	6.3 x 6.3	Amkor	Delivered
10 x 10	7 x 7	0.4	88	0.85	1	NiPdAu	8.1 x 8.1	Amkor	Delivered
10 x 10	4	0.5	132	0.85	2	Matte Sn	6.9 x 6.9	Amkor	Delivered
12 x 12	6	0.5	164	0.85	2	Matte Sn	8.9 x 8.9	Amkor	Delivered
10 x 10	6	0.5	132	0.85	2	Matte Sn	6.9 x 6.9	Amkor	Delivered
12 x 12	8	0.5	164	0.85	2	Matte Sn	8.9 x 8.9	Amkor	Delivered
7 x 7	1.11 x 1.11	0.5	92	0.9	2	NiPdAu	4.8 x 4.8	ASAT	Delivered
7 x 7	4.55 x 4.55	0.5	92	0.9	2	NiPdAu	4.8 x 4.8	ASAT	Delivered
10 x 10	4.11 x 4.11	0.5	140	0.9	2	NiPdAu	7.8 x 7.8	ASAT	Delivered
10 x 10	7.55 x 7.55	0.5	140	0.9	2	NiPdAu	7.8 x 7.8	ASAT	Delivered
1 (SOT891)	0.43 x 0.64	0.35	6	0.5	1	NiPdAu	N/A	NXP	Delivered
1 (XSON6)	0.43 x 0.64	0.3	6	0.5	1	NiPdAu	N/A	NXP	Delivered
3 (XSON38)	0.5 x 0.5	0.35	38	0.5	2 (each side)	NiPdAu	N/A	NXP	Delivered
12	7	0.5	236	0.85	3	NiAu	8.8 x 8.8	ASE	Delivered
4 x 4	2 x 2	0.4	32	1	1	NiPdAu	2.8 x 2.8	TI	Delivered

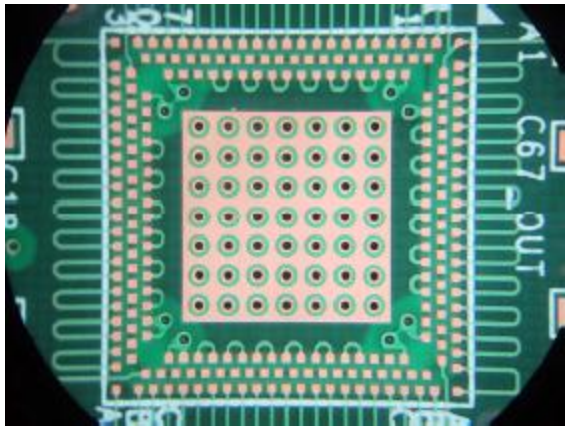
Test Board Layout (Top Side)

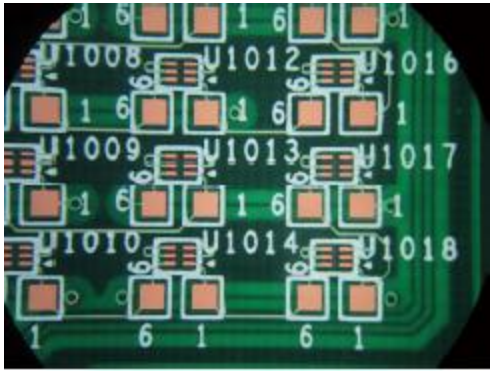
HDP USER GROUP INTERNATIONAL, INC.®



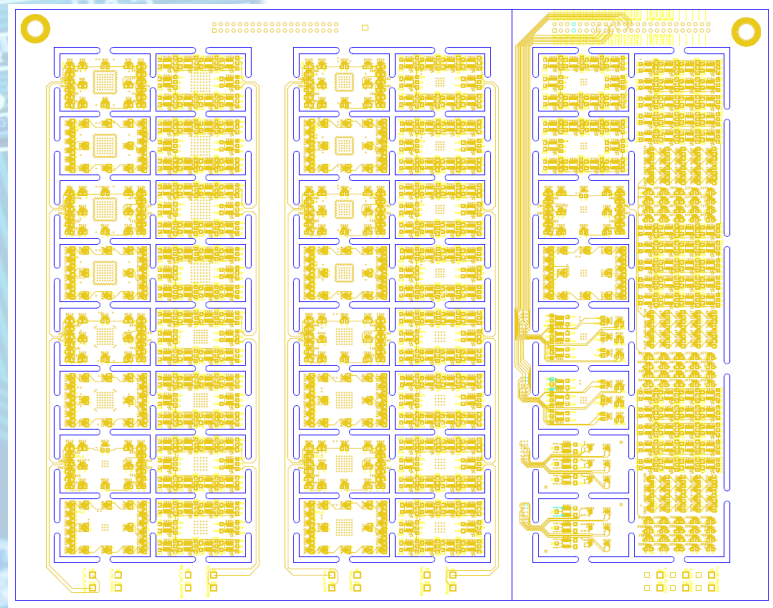


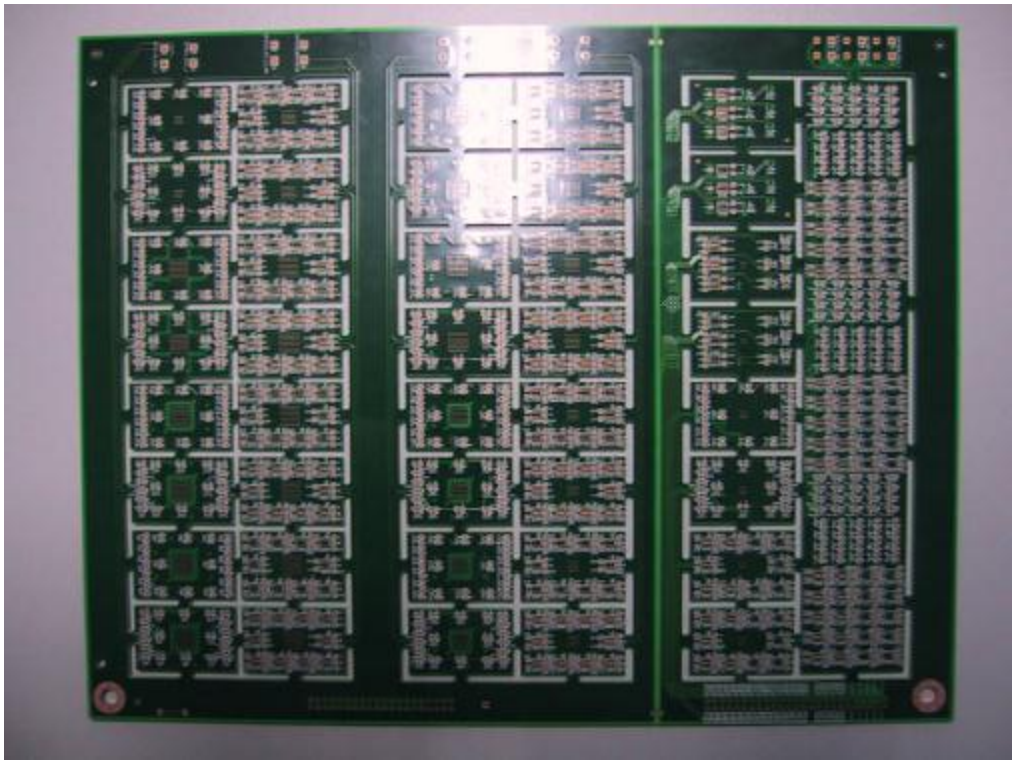






Test Board Layout (Bottom Side)





Board Materials

- 8 layer, 2.36 mm (93 mil) thick
  - One layer HDI
  - Via-in-Pad (VIP) design used for TLA (dual row) and aQFN (3 row)
- Cu OSP surface finish
- High Tg FR4

Assembly Process Evaluation

- Process Selection
  - Pb-free
  - No clean
- Stencil Design
- Reflow profile
- Inspection
- Rework

Assembly Process for Fine Pitch QFN

- Will support building large quantity of 0.3/0.35 mm pitch QFN parts to assess the assembly yield – done on the bottom side.
- Will use the combined continuity measurement and x-ray inspection to detect opens and shorts and to assess assembly yield to the 100 dppm solder joint level.

(Source: Amkor)

Board Level ATC Testing

- Two temperature profiles to be used
  - 0 to 100 deg. C – 10 mins. dwell time
  - 0 to 100 deg. C – 60 mins. Dwell time